Module - 1.

Transistor Biasing.

Prototype - Basic circuit design.

Transistor bias - The process of setting the operating Point of a transistor for its stable & reliable performance.

Different types of bias
→ Base bias — used in design of switching circuits
→ Emitter " — " " " " amplifying "

Voltage Divider Bias (self Bias ~~or Base Bias~~)

The bias circuit that contains voltage divider (R1 & R2) at the base is called voltage-divider bias (VDB).

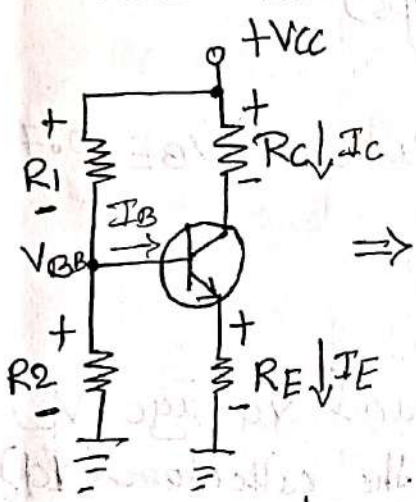


Fig1. VDB circuit

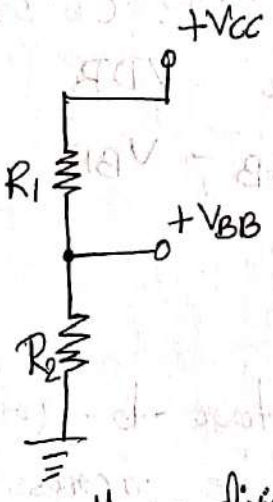


Fig2. voltage divider Circuit

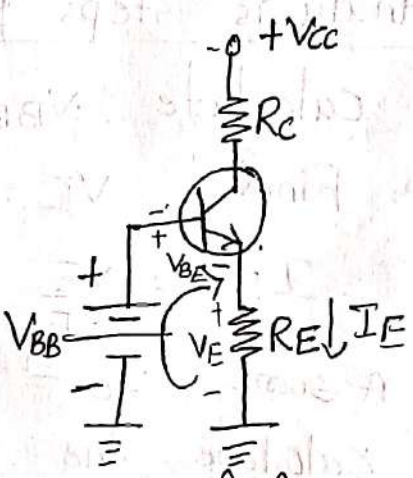


Fig.3 simplified VDB Circuit.

→ Fig. 1 shows voltage divider bias circuit.
→ R1 & R2 divides the voltage at the base.
→ Base current IB is very small
→ we can open the transistor mentally & equivalent of voltage divider circuits looks like as in fig2.
→ Base supply voltage VBB is given by

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$

By applying KVL at the loop in fig.3 (Base-emitt

→ $V_{BB} - V_{BE} - V_E = 0$

$$\boxed{V_E = V_{BB} - V_{BE}}$$

$$V_E = I_E R_E$$

$$\boxed{I_E = \frac{V_E}{R_E}}$$

$I_E = I_C + I_B$ I_B is very small

$\therefore I_C \cong I_E$

$V_C = V_{CC} - I_C R_C$

Collector to Emitter voltage

$$\boxed{V_{CE} = V_C - V_E}$$

Analysis steps for VDB (6 steps)

1. Calculate V_{BB} for VDB.
2. Find $V_E = V_{BB} - V_{BE}$ where $V_{BE} = 0.7$.
3. $I_E = \frac{V_E}{R_E}$
4. Assume $I_C \cong I_E$
5. Calculate the collector-to-ground voltage (V_C) by subtracting voltage across the collector ($I_C R_C$) resistor from collector supply (V_{CC})
6. Calculate $V_{CE} = V_C - V_E$.

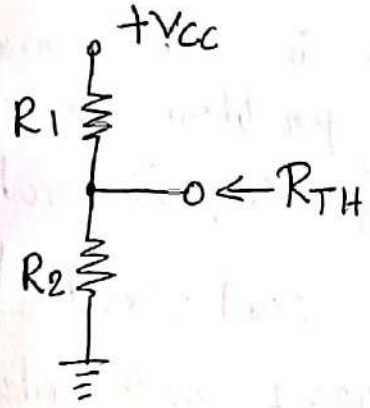
Accurate VDB analysis

→ It is the one in which the voltage divider appears stiff to the input resistance of the base

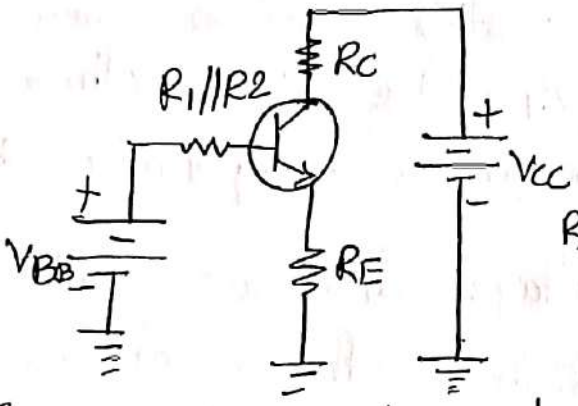
Stiff voltage source $R_S < 0.01 R_L$.

→ R_S must be 100 times R_L.

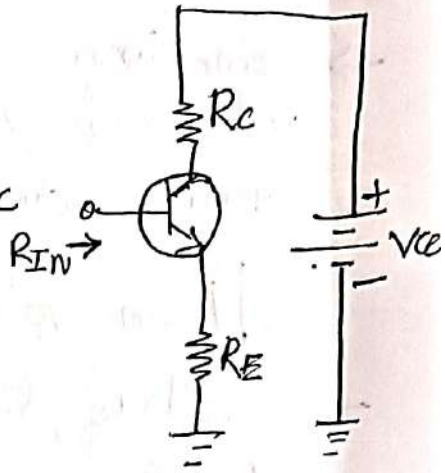
→ we have VDB circuit as,



Thevenin resistance.



Equivalent circuit



Input resistance of base.

→ Thevenin resistance $R_{TH} = R_1 || R_2$ it act as source resistor R_S

→ voltage divider sees a load resistance of R_{IN} so R_L here is nothing but R_{IN}

→ voltage divider to appear stiff to the base it has to follow 100:1 rule.

$$R_S < 0.01 R_L.$$

$$\boxed{R_1 || R_2 < 0.01 R_{IN}}$$

$R_S = R_{TH} = R_1 || R_2$

$R_L = R_{IN}$

well designed VDB circuit will satisfy this condition.

Stiff voltage divider.

→ If Transistor has a current gain (β_{dc}) of 100.

$I_C = (\beta_{dc}) \overset{or}{100} I_B$, $I_E = (\beta_{dc}) \overset{or}{100} I_B$.

→ From the base R_E appears to be 100 times larger.

$\therefore R_{IN} = \beta_{dc} R_E$

$$\boxed{\text{Stiff voltage divider: } R_1 || R_2 < 0.01 \beta_{dc} R_E}$$

→ Whenever possible, a designer selects circuit values to satisfy this 100:1 rule. It will produce an ultrastable Q-point

→ Sometimes a stiff design results in such a small values of R_1 & R_2 that other problem arises.

→ Many designers compromise by using this rule.

Firm voltage divider: $R_1 \| R_2 < 0.1 \beta_{dc} R_E$

→ voltage divider that satisfies 10:1 rule called as firm voltage divider.

→ VDB circuit has a reasonably stable Q point.

→ If we want a more accurate value of emitter current.

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + (R_1 \| R_2)/\beta_{dc}}$$

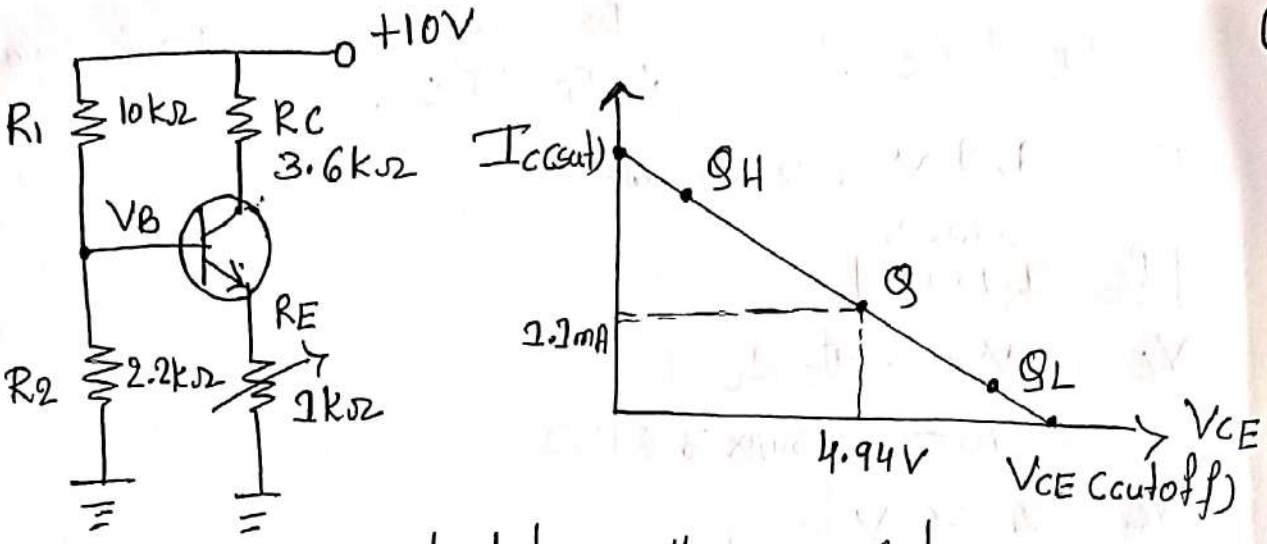
→ above equation will improve the analysis but it is a complicated formula.

VDB and Load Line and Q point

→ As we have stiff voltage divider circuit, to analyze load line & Q point, V_E is held constant. i,e $V_E = 1.1V$.

→ If we have $V_{CE} = 4.94V$ & $I_C = 1.2mA$

→ If we plot it on the graph will get the Q point as following.



Calculating the Q point

- Voltage divider bias is the modification of emitter bias.
- If current gain (β_{dc}) changes Q point ~~at~~ will not change (move).
- One way to move the Q point is by varying the emitter resistor R_E.

Condition-1. If R_E changed to 2.2 kΩ, I_C or I_E decreases to.

$$I_E = \frac{V_E}{R_E} = \frac{1.1\,V}{2.2\,k\Omega} = 0.5mA, \quad \text{Consider } V_E = 1.1\,V$$

The voltage V_C changes

$$V_C = V_{CC} - I_C R_C$$
$$= 10 - (0.5mA)(3.6k\Omega)$$
$$\boxed{V_C = 8.2V}$$

&

$$V_{CE} = V_C - V_E$$
$$= 8.2 - 1.1$$
$$\boxed{V_{CE} = 7.1V}$$

- Q shifts ~~to~~ now Q is called Q_L with co-ordinates (0.5mA, 7.1V) (V_{CE}, I_C).
- Condition-2 If R_E decreased to 510 Ω, I_E or I_C increases to:

$I_E \cong I_C$.

$I_E = I_C + I_B$ I_B is small

$\therefore I_E \cong I_C$.

$$I_E = \frac{1.1\ V}{510\ \Omega} = 2.15\ mA$$

$\boxed{I_C = 2.15\ mA}$

$V_C = V_{CC} - I_C R_C$

$= 10 - 2.15mA \times 3.6k\Omega$

$V_C = 2.26\ V$.

and

$V_{CE} = V_C - V_E$

$= 2.26 - 1.1$

$\boxed{V_{CE} = 1.16\ V}$

→ Q-point shifts to a new position at Q_H with co-ordinates of 2.15mA & 1.16V (2.15mA, 1.16V) (I_C, V_{CE})

→ V_{CC}, R_1, R_2 & R_C changes $I_{C(sat)}$ & $V_{CE(cutoff)}$

→ Designer keeps the above value constant.

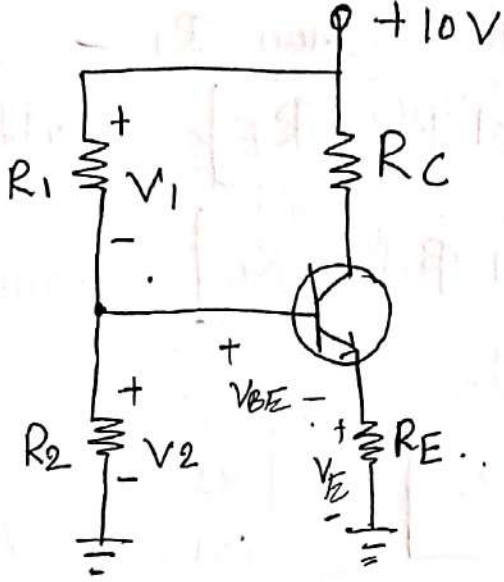
→ R_E is varied to set the Q point.

→ If R_E is too large Q point moves in to the cutoff point.

→ If R_E is too small, the Q point moves in to saturation.

VDB Design Guideline

→ VDB circuit & concept is the simple way to establish a stable Q-point.



VBB design

For the circuit we should know Vcc., Bdc. & range for the transistor.

Step-1. Emitter voltage must be approximately one-tenth of supply voltage.

$$V_E = 0.1\ V_{CC}$$

Step-2 Calculate R_E for I_C to set up I_C

$$R_E = \frac{V_E}{I_E}$$

Step-3 To have Q-point at mid of the DC load line, $0.5 V_{CC}$ appears across collector-emitter terminals. The remaining $0.4 V_{CC}$ appears across the collector resistor,

$$\therefore \quad R_C = 4 R_E$$

Step-4. Design stiff voltage divider using 100:1 rule

$$R_{TH} \leq 0.01\ B_{dc}\ R_E$$

Firm voltage divider rule can be used

Usually R_2 is smaller than R_1

$\therefore$ $\boxed{R_2 \leq 0.01 \beta_{dc} R_E}$ stiff rule

$\boxed{R_2 \leq 0.1 \beta_{dc} R_E}$. Firm rule.

step-5 Finally calculate

$$\boxed{R_1 = \frac{V_1}{V_2} R_2}$$

By applying KVL to BE

$\boxed{V_2 = V_{BE} + V_E}$

$\boxed{V_1 = V_{CC} - V_2}$

Two-Supply Emitter Bias (TSEB)

→ Some electronic equipment has a power supply that produces both positive and negative supply voltages.

→ Fig shows a transistor circuit with two supplies: +10V & −2V.

→ This circuit is derived from emitter bias.

Fig: Two supply emitter bias.

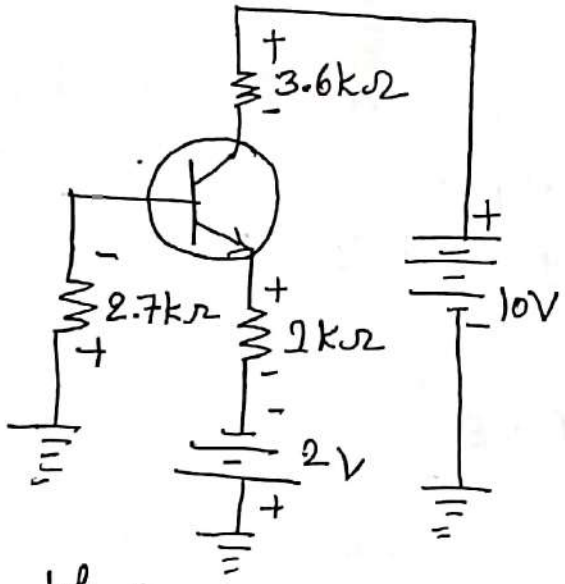
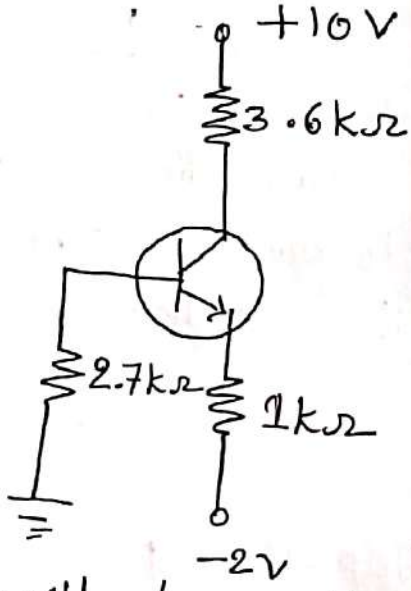


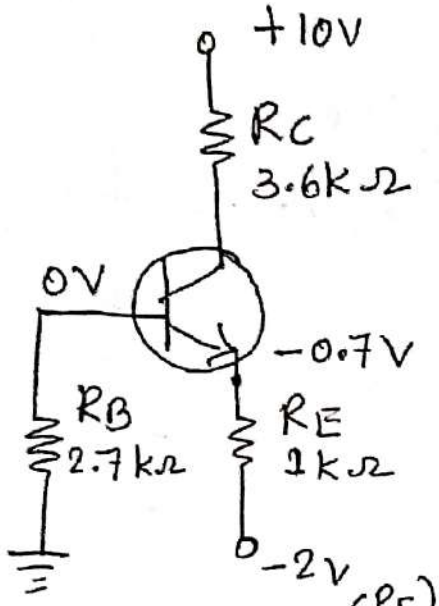
Fig: Redrawn TSEB Circuit.



→ Simplified TSEB is a circuit without battery.

→ When this type of circuit is correctly designed, the base current will be small & base voltage is 0V.

The voltage across emitter ~~VE = -0.7V~~ -0.7V



- Emitter resistance (R_E) is very important to find I_E
- apply ohm's law to the emitter resistor.
- voltage across emitter resistor is the difference between low negative & high negative voltage.

∴ voltage across R_E i,e V_{RE} is given by

$$V_E = V_{RE} = -0.7V - (-2V) = 1.3V$$

calculate I_E using ohm's law

$$I_E = \frac{V_{RE}}{R_E} = \frac{1.3}{2k} = 1.3mA$$

$I_C \cong I_E$ so the same current flows through 3.6kΩ & produces the voltage drop that we substract from +10V as.

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 10 - (3.6k)(1.3mA)$$

$$V_C = 5.32V$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = 5.32 - (-0.7)$$

$$V_{CE} = 6.02V$$

→ Two supply emitter bias also satisfies the stiff voltage rule

$\therefore R_B < 0.01 \beta_{dc} R_E$.

In this case, simplified equations for analysis are

$V_B \approx 0$.

apply KVL between emitter & ground.

$I_E = \frac{V_{EE} - 0.7V}{R_E}$ $(-0.7V - I_E R_E + V_{EE} = 0)$.

$V_C = V_{CC} - I_C R_C$.

$V_{CE} = V_C + 0.7V$ $(V_{CE} = V_C - V_E)$ but $V_E = -0.7$.

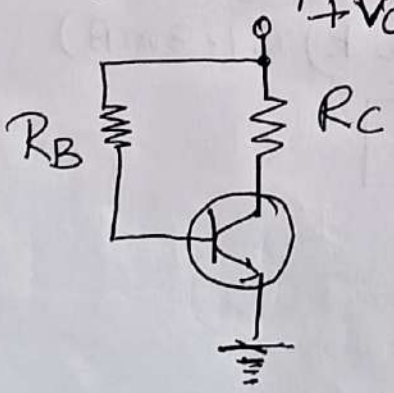
→ There is a problem with simplified method that a small voltage across the base resistor. due to which a small base current flows through the resistor, a negative voltage exist between base & ground.

→ In well-designed circuit V_B is less than $-0.1V$.

Other types of Bias.

Emitter-Feedback Bias.

→ In a base bias circuit like below, the Q point moves all over the load line with transistor replacement & temperature change.



$I_B = \frac{V_{BB} - V_{BE}}{R_B}$

$I_C = \beta I_B$

$I_C = \frac{V_{CC} - V_{CE}}{R_C}$.

> In order to stabilize the Q-point the circuit was designed called emitter-feedback bias. emitter resistors added to the circuit.

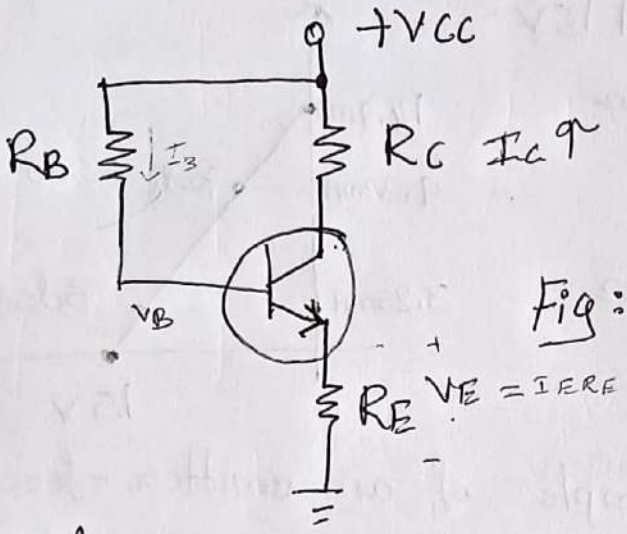


Fig: Emitter-Feedback Bias.

$\uparrow I_C = I_E + I_B \downarrow$
$\uparrow V_B$

Basic Idea.

→ If I_C increases V_E increases ($V_E = I_E R_E$)
$I_E \uparrow = I_C$.

→ When V_E increases V_B also increases ($V_{BE} = V_B - V_E$)

→ More V_B means less voltage across R_B.

→ Less I_B which opposes original increase ($V_B = I_B R_B$)
in I_C

→ It is called feed back (change in emitter voltage is fed back to base).

→ It is a negative feed back as it opposes the original change in I_C.

→ The movement of Q-point is still too large.
hence never became popular.

→ Equations for analyzing the emitter-feedback bias.

$$I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{dc}}$$

$I_E \approx I_C = \beta I_B$

$I_B = \frac{I_E}{\beta}$

$V_E = I_E R_E$

$V_B = V_E + 0.7V$ ($V_{BE} = V_B - V_E$; $V_B = V_E + V_{BE}$)

$V_C = V_{CC} - I_C R_C$

Fig: Example of emitter feedback bias

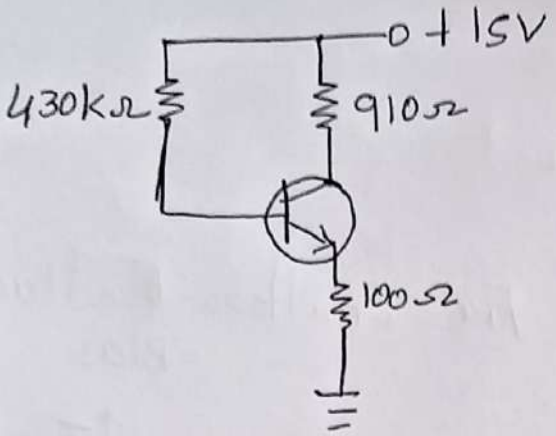
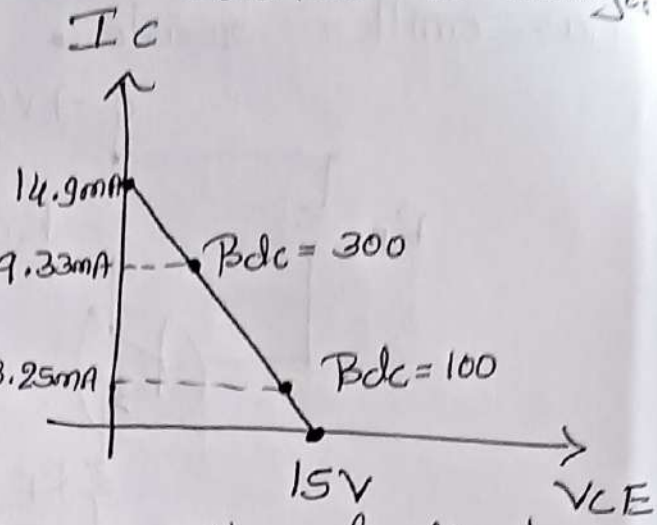


Fig: Q point is sensitive to change.



→ Fig shows an example of an emitter-feedback bias circuit.

→ Fig shows the load line and the Q-point for two different current gains.

→ A 3:1 variation in current gain produces a large variation in collector current.

→ The circuit is not much better than base bias.

Collector-Feedback Bias.

→ It is another attempt at stabilizing the Q-point.

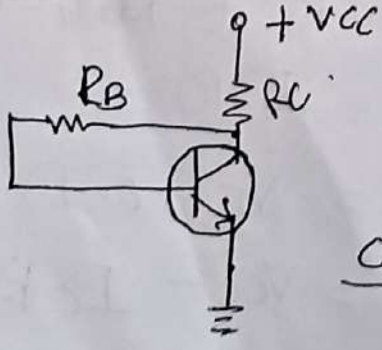
→ Here voltage is feedback to the base to neutralize the change in I_C.

→ If I_C ↑ increases; V_C decreases ($V_C = V_{CC} - I_C R_C$)

→ which decreases the voltage across base resistor.

& decreases I_B which opposes the orginal increase in I_C.

→ It is a negative feedback.



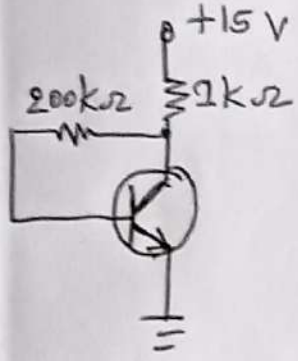
Collector-feedback bias

→ Equations for analysing collector-feedback bias.

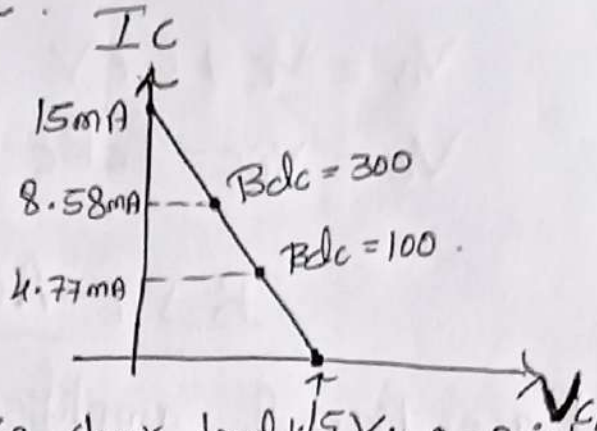
$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B / \beta_{dc}}$$

$$V_B = 0.7V$$

$$V_C = V_{CC} - I_C R_C$$



→ Fig shows an example of collector-feedback bias.



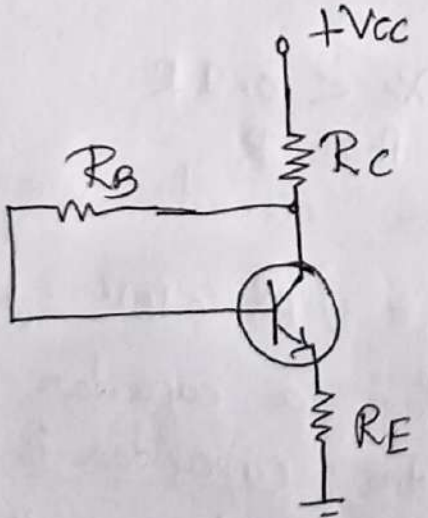
→ Fig shows load line & Q-point for 2 different current gains.

→ 3:1 variation in current gain produces less variation in collector current than emitter-feedback.

→ It is more effective than emitter-feedback bias in stabilizing the Q-point. used in practice as it is simple.

Collector- and Emitter-Feedback bias

→ The basic idea is to use both emitter and collector feedback to try to improve the operation.



→ It combines both emitter & collector feedback bias

→ Equations for analysing

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_E + R_B + \beta_{dc}}$$

$$V_E = I_E R_E$$

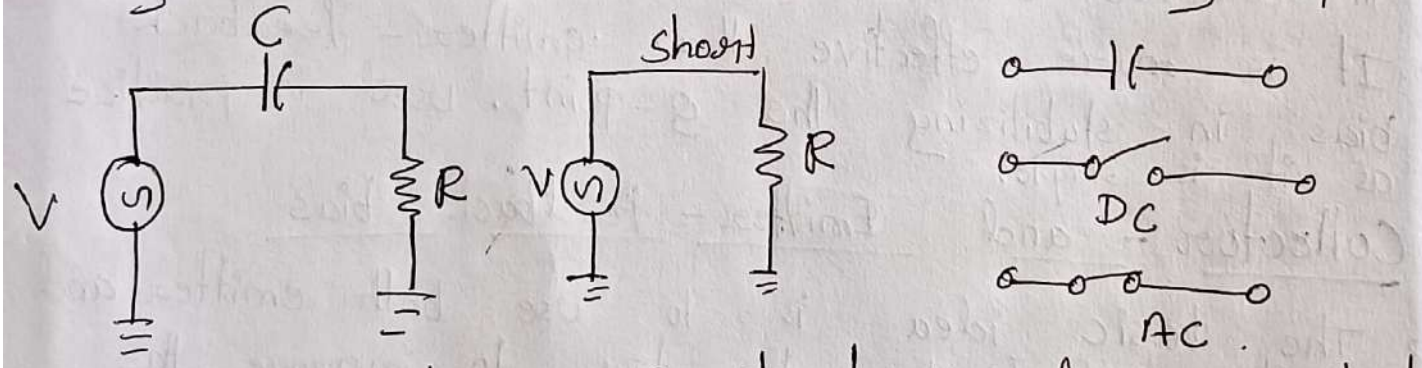
$$V_B = V_E + 0.7\,V$$

$$V_C = V_{CC} - I_C R_C .$$

BJT AC models.

Base biased amplifier.

→ coupling capacitor - couples or transmitts the ac signal to the resistor without disturbing Q-point.



Coupling capacitor . AC short . dc open & ac short.

Good coupling: $X_C < 0.1R$.

X_C → 10 times smaller than R.

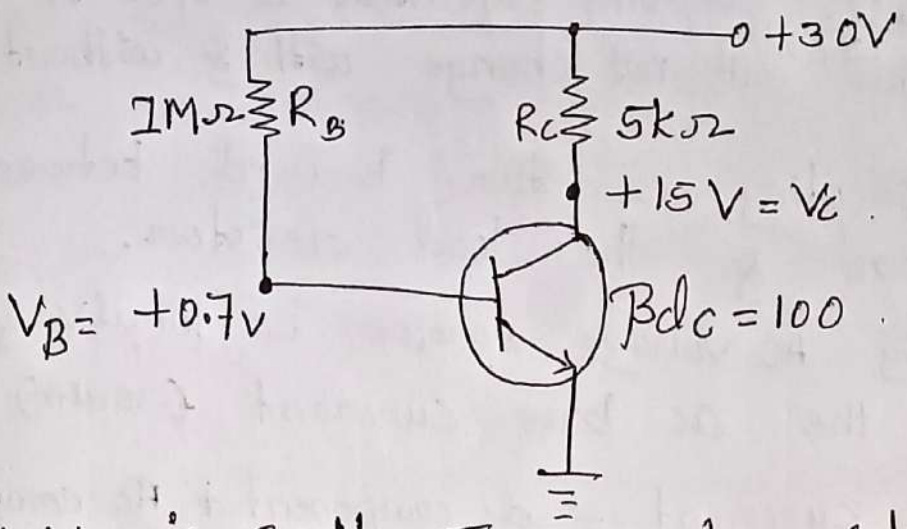
→ So for coupling capacitor circuit we can apply

$$Z = \sqrt{R^2 + X_C^2} = \sqrt{R^2 + (0.1R)^2} = \sqrt{R^2 + 0.01R^2} = 1.005R.$$

Two approximations for a capacitor.

1. For dc analysis the capacitor is open.
2. For ac " " " " shorted.

→ Fig shows a base biased circuit.



→ as V_B is small. I_B can be calculated as

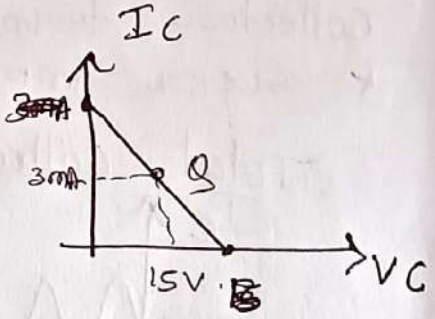
$$I_B = \frac{V_{CC}}{R_B} = \frac{30}{1M}$$

$$\boxed{I_B = 30\,\mu A}$$

→ $I_C = \beta_{dc} I_B$

$I_C = 30\mu \times 100$

$$\boxed{I_C = 3mA}$$



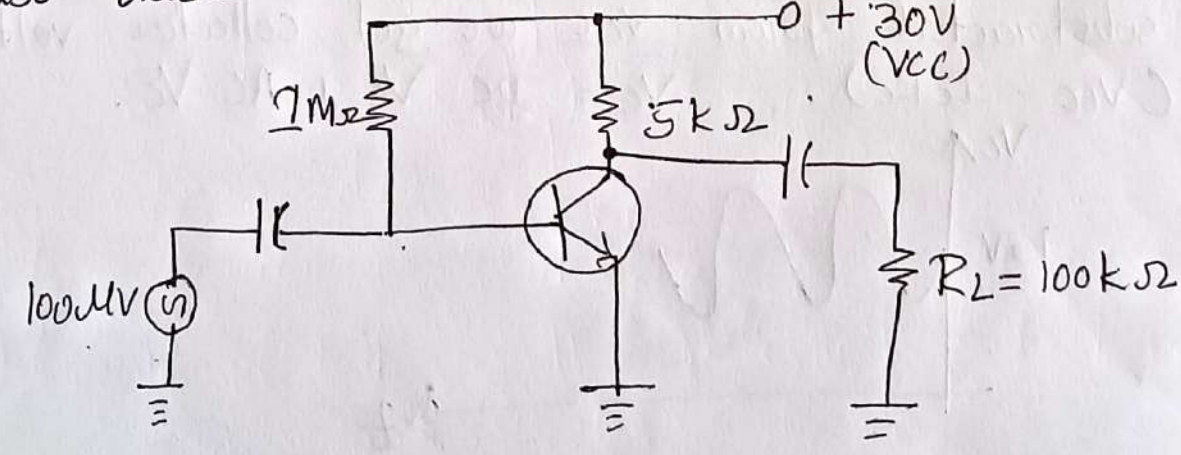
→ $V_C = V_{CC} - I_C R_C$.

$= 30 - 3m \times 5k$.

$$\boxed{V_C = 15V}$$

→ So, Q point is located at 3mA & 15V

→ Fig shows how to add components to build base biased circuit as an amplifier.

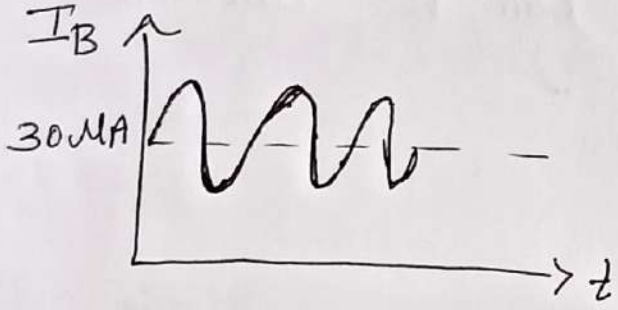


→ A coupling capacitor used between an ac source and the base. Coupling capacitor is open to DC so DC bias (Q point) will not change with & without capacitor.

→ Another coupling capacitor is used between the collector & the load resistor.

→ In above fig AC voltage source is 100μV & it produces the ac base current ~~(30μA)~~

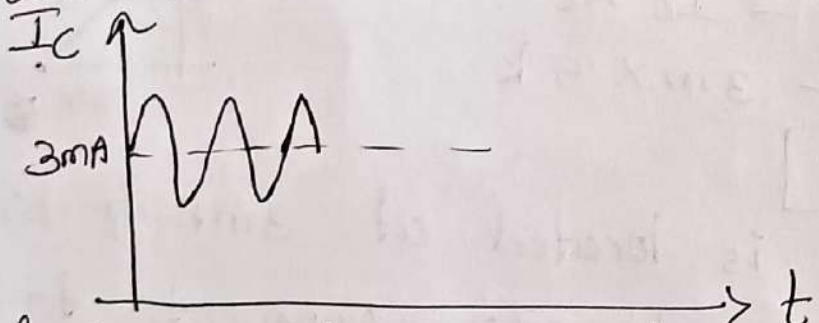
→ Total base current = dc component + Ac component.



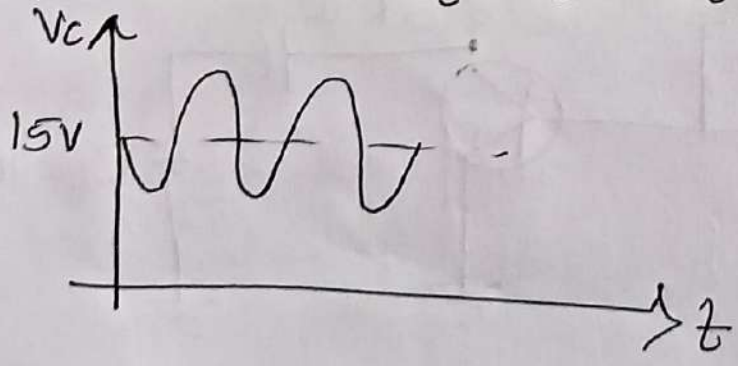
→ on +ve half cycle ac base current adds to dc " "
→ on -ve half cycle ac base current substract to dc " "

→ This ac base current amplified by the transistor collector terminal (as it has current gain $\beta dc = 100$.) & super imposed with dc collector current (3mA)

Total collector current = dc I_C + Ac I_C.

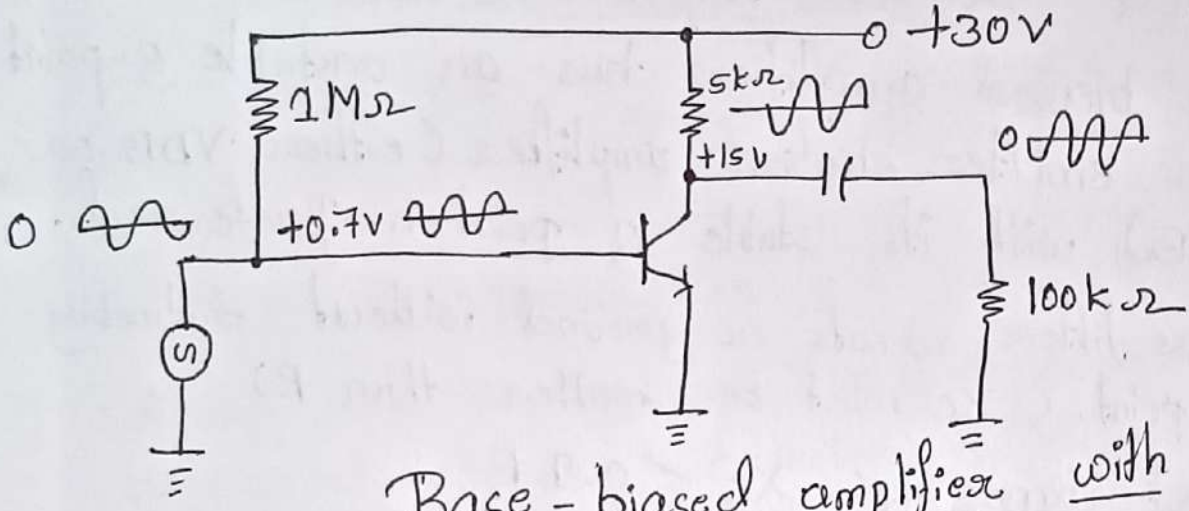


→ Amplified collector current I_C flows through R_C, it produces voltage across R_C. when this voltage is substracted from V_{CC} we get collector voltage V_C ($V_{CC} - I_C R_C$). V_C = DC V_C + AC V_C.



→ On the positive half cycle of ac base current (I_B), the I_C increases & produces more voltage across R_C. Means there is a less voltage between collector & ground hence V_C is -ve.

→ On the negative half cycle, I_C decrease → Less voltage across R_C, V_C increases hence +ve.

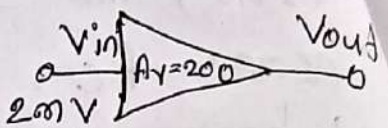


Base-biased amplifier with waveforms

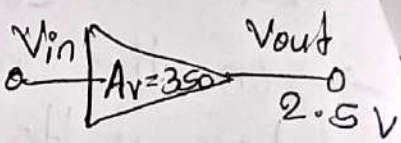
→ source voltage is 100mV. AC.
→ It is super imposed with DC base voltage 0.7V.
→ variation in V_B produces variation in I_B, I_C & V_C.
→ the total collector voltage is an inverted sine wave superimposed on dc collector voltage of +15V.
→ Output coupling capacitor blocks dc component of V_C & it couples ac collector voltage (ve) to the load resistor. Load voltage is pure ac.

Voltage gain → $A_v = \frac{V_{out}}{V_{in}}$

Output voltage → $V_{out} = A_v V_{in}$



Input voltage → $V_{in} = \frac{V_{out}}{A_v}$



Emitter Biased Amplifier (VDB or TSEB)

→ Base biased amplifier has an unstable Q-point.

→ Hence emitter-biased amplifier (either VDB or TSEB) with its stable Q point is preferred.

→ A bypass filter creats ac ground without disturbing its Q point. (X_C must be smaller than R).

Good bypassing: $X_C < 0.1R$.

VDB Amplifier with waveforms

→ Fig shows VDB amplifier.

→ To calculate dc voltage & current mentally open all capacitor.

→ The DC values for this circuit are.

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{10 \times 2.2}{12.2} = 1.8V.$$

$\boxed{V_B = 1.8V}$

$V_E = V_B - V_{BE}$ $(V_{BE} = V_B - V_E)$

$V_E = 1.8 - 0.7$

$\boxed{V_E = 1.1V}$.

$$I_E = \frac{V_E}{R_E} = \frac{1.1}{1k} = 1.1mV.$$

$\boxed{I_C = 1.1mV}$

$I_E \cong I_C$.

$V_C = V_{CC} - I_C R_C$.

$V_C = 10 - 1.1\text{m} \times 3.6\text{k}$.

$\boxed{V_C = 6.04\ V}$

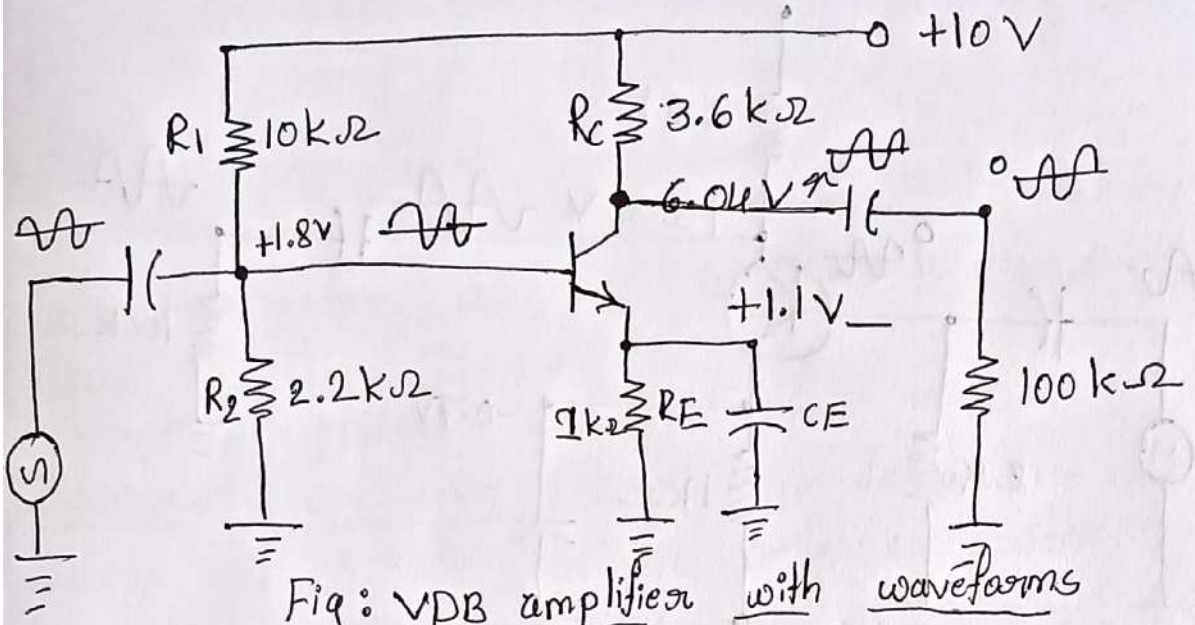


Fig: VDB amplifier with waveforms

-> Along with coupling capacitor [(between source & base) and C between collector & R_L)] a bypa capacitor must be used between emitter and grou to get largeor voltage gain.

> 100μV ac source voltage is a small sinusoid voltage with an average value of zero.

> Base voltage is superimposed Ac & DC (100μV ac + 1.8V dc).

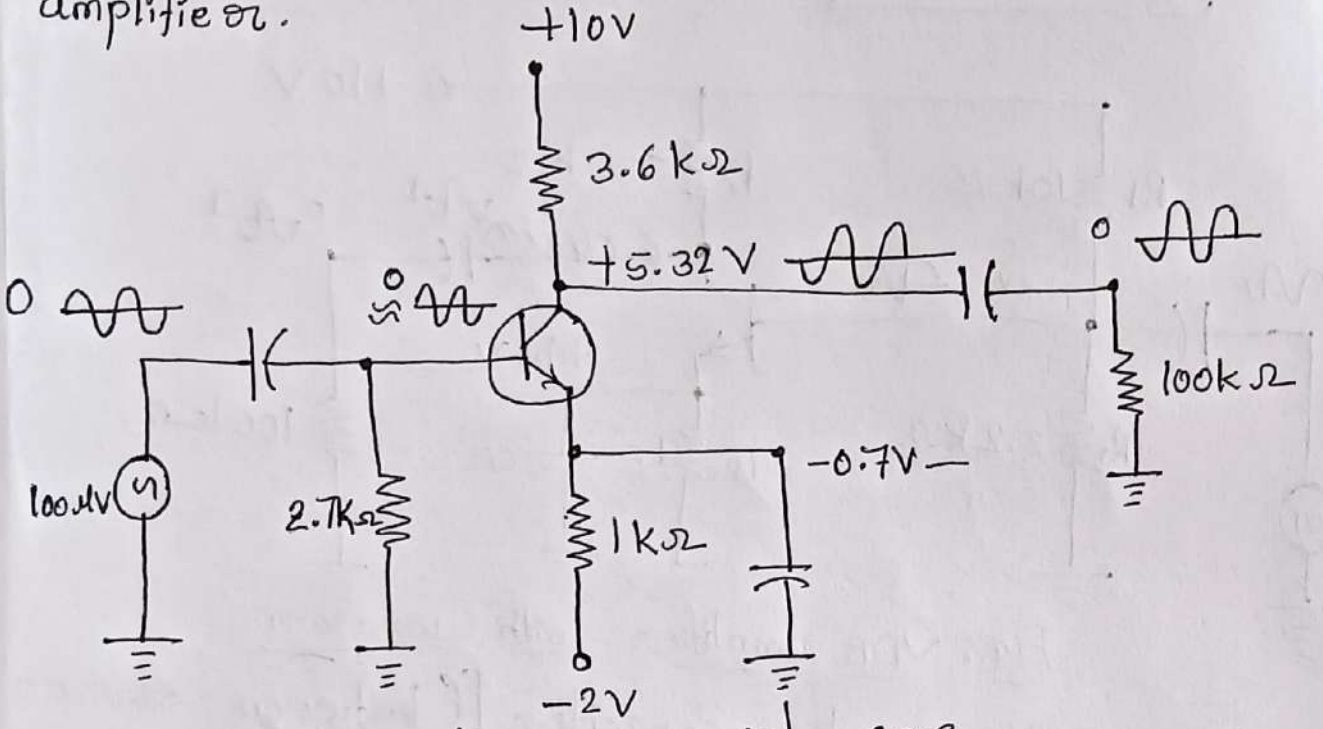
> Collector voltage V_c is an amplified & inverted ac voltage superimposed on dc (V_C = Ac amplified + 6.04 DCV).

Load voltage is the pure ac voltage which is same as collector ac voltage.

Emitter voltage is pure dc as it has bypass capacitor.

TSEB (Circuit) amplifier with waveforms

→ Fig shows a two-supply emitter bias (TSEB) amplifier.



→ DC voltage for Q-point are

$V_B \cong 0$.

$V_{BE} = V_B - V_E = 0 - 0.7$

$V_E = -0.7V$

$\boxed{V_E = -0.7V}$

$I_E = \frac{V_E}{R_E} = \frac{0.7 + 2}{1k} = 1.3mV$

$\boxed{I_C = 1.3mV}$

$I_E \cong I_C$.

$V_C = V_{CC} - I_C R_C$.

$= 10 - [(1.3m)(3.6k)]$

$\boxed{V_C = 5.32\ V}$

→ Fig has two coupling capacitor & one bypass capacitor.

→ The ac source voltage is small ac voltage 100μV.

→ Base ac component voltage is an superimposed ac & DC voltage (DC = 0V).

→ Collector voltage is an inverted voltage super imposed on dc collector voltage (5.32V)

→ Load voltage is the same ~~apti~~ amplified signal with no DC component.

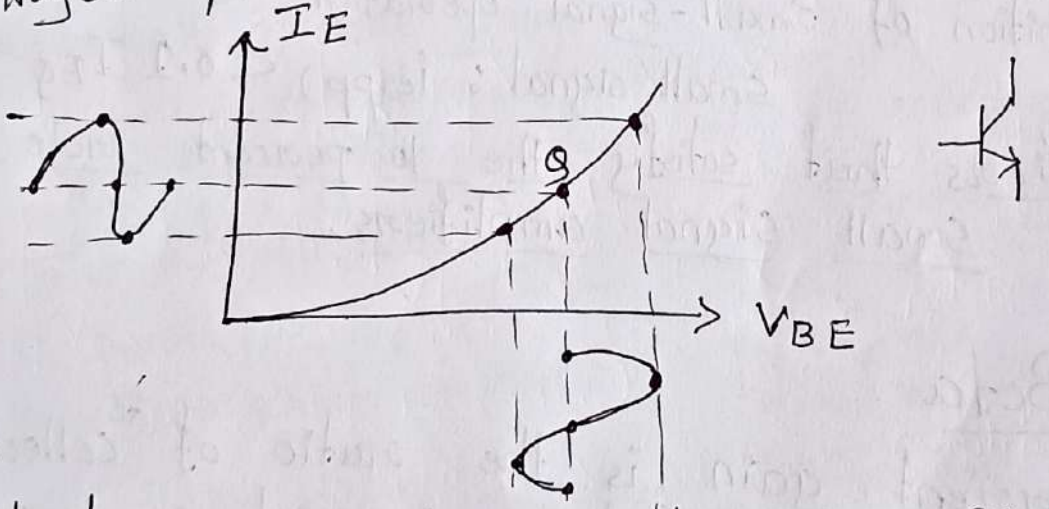
→ Bypass capacitor is used to increase the voltage gain & to maintain ac ground.

Small-Signal operation.

→ When an ac voltage is applied to the base of transistor, an ac voltage appears across base emitter diode.

→ Graph is plotted V_{BE} Vs I_E for analysis.

Instantaneous operating point - The total base-emitter voltage of fig is an ac voltage centered on a dc voltage. The size of the ac voltage determines instantaneous movement of Q point. Larger ac base voltages produces large variations & vice versa.

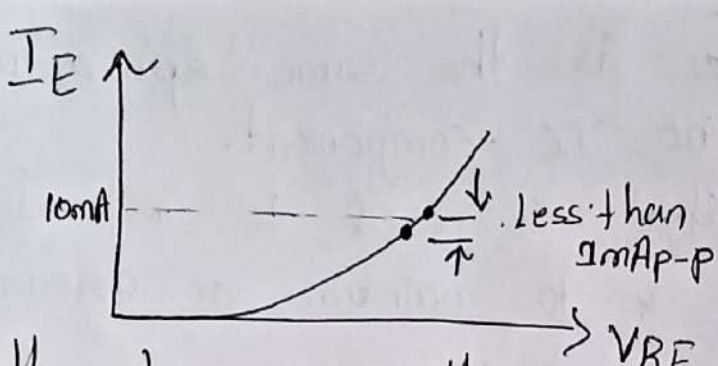


Distortion - AC I_E is not same as AC V_{BE} Positive half cycle of AC emitter current (I_E) is elongated (stretched) and negative half cycle is compressed. This stretching and compressing of AC half cycle is called distortion.

Reducing distortion

→ One way of reducing the distortion is keeping the V_{BE} as small as possible.

→ Smaller the V_{BE} smaller the I_E, more linear the graph.



→ if the base ac voltage is a small enough sine wave, the ac emitter current will be small sine wave with no noticeable stretching or compression of half cycle.

→ $I_E = I_{EQ} + i_e$

I_E = Total emitter current
I_{EQ} = The DC emitter "
i_e = the ac " "

→ To minimize the distortion, the peak-to-peak value of i_e must be small compared to I_{EQ}.

Definition of small-signal operation is

Small signal : $i_{e(pp)} < 0.1\, I_{EQ}$

→ Amplifiers that satisfy the 10 percent rule are called small signal amplifiers.

AC Beta

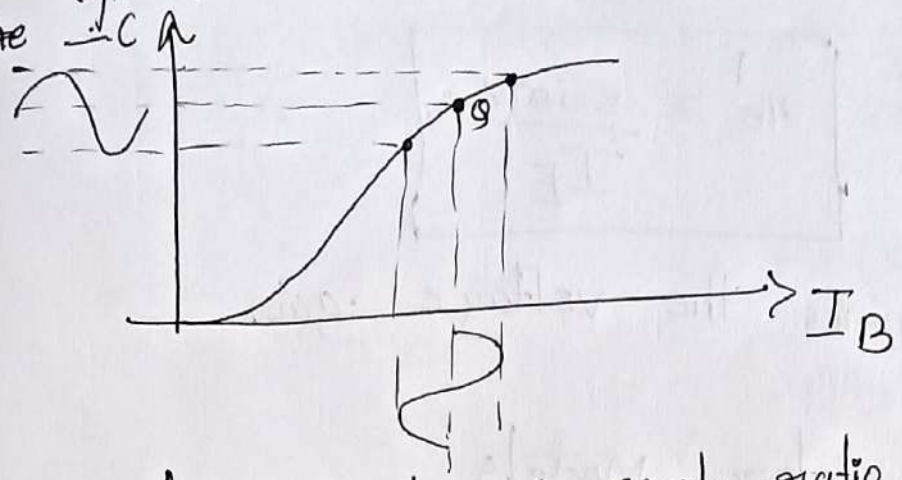
→ dc current gain is the ratio of dc collector current to the dc base current. represented by B_{dc}

$$B_{dc} = \frac{I_C}{I_B}$$

→ ac current gain is the ratio of ac collector current to the ac base current called ~~as~~ AC Beta

$$\beta = \frac{i_c}{i_b}$$

If we plot the graph I_B Vs I_C. we get



Ac current gain equals ratio of changes.

> dc current gain depends on the location of the Q point.

> In fig the ac signal uses only a small part of the graph on both sides of the Q-point.

> Because of this, the value of the ac current gain is different from the dc current gain, which uses almost all of the graph.

> β equals the slope of the curve at Q-point

> β depends on the amount of dc collector current.

Note - To differentiate ac & dc quantities.

ac quantities - lower letters & subscripts are used. → i_e, i_c, i_b ; v_e, v_c, v_b ; v_{be}, v_{ce}, v_{cb}.

DC quantities - to Upper case letters & subscripts are used → I_E, I_C, I_B ; V_E, V_C, V_B ; V_{BE}, V_{CE}, V_{CB}.

AC Resistance of the Emitter Diode.

ac emitter resistance of the emitter diode r_e'

$$r_e' = \frac{v_{be}}{i_e}.$$

→ with solid-state physics & calculus, it is r_e' is given by

$$r_e' = \frac{25mV}{I_E}$$

→ r_e' determines the voltage gain.

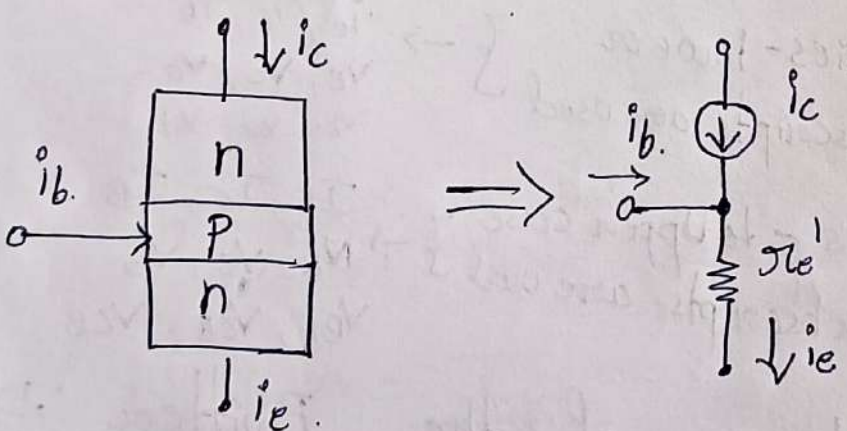
Two Transistor Models

→ Transistor model is an ac equivalent circuit of a transistor. used to analyse ac operation of a transistor amplifier.
→ There are two transistor models.

1. T model
2. π model.

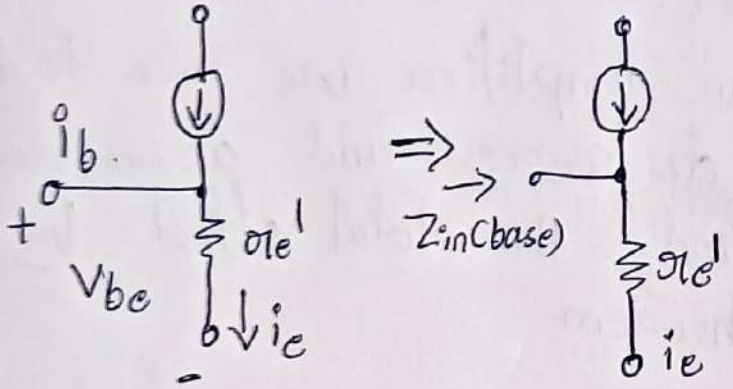
T- Model (Ebers - Moll model).

→ One of the earliest model.
→ called as Ebers - Moll model also.
→ the name T is used as it has T shape.



→ The model circuit looks as in fig.
→ the emitter diode of a transistor acts like an ac resistance (r_e')
→ Collector diode act like a current source (i_c)

→ when analysing a transistor amplifier, we can replace each transistor by T-model and calculate the value of r_e' and other ac quantities.



$$Z_{in(base)} = \frac{V_{be}}{i_b}$$

apply KCL to B-E loop

$$V_{be} = i_e r_e'$$

$$\therefore Z_{in(base)} = \frac{i_e r_e'}{i_b}$$

as $i_e \approx i_c$

$$Z_{in(base)} = \frac{i_c r_e'}{i_b} = \beta r_e'$$

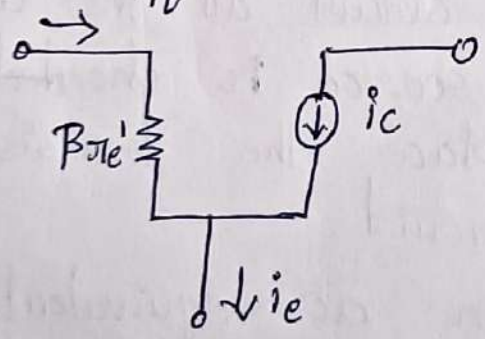
β → current gain

→ Input impedance of the base is equal to the ac current gain times the ac resistance of the emitter diode.

2. <u>Π- model</u>.

→ It is the virtual representation of $Z_{in(base)} = \beta r_e'$

→ It is easy to use than the T-model because input impedance is seen clearly in Π model.



→ Most of the time Π model is used for analysis.

Analysing an amplifier.

→ Amplifier analysis is complicated because both dc & ac sources are available in the same circuit.

→ To analyse an amplifier we have to calculate the effect of dc sources and ac sources seperately & then find the total effect by super position theorem.

1. DC Analysis

→ DC analysis calculate the dc voltages & currents like V_{BE}, I_B, I_C & V_{CE}

→ To draw the DC equivalent circuit open all the capacitors. then the remaining circuit is known as DC equivalent circuit of ~~of~~ an amplifier.

AC Analysis

→ Ac analysis is done after dc analysis.

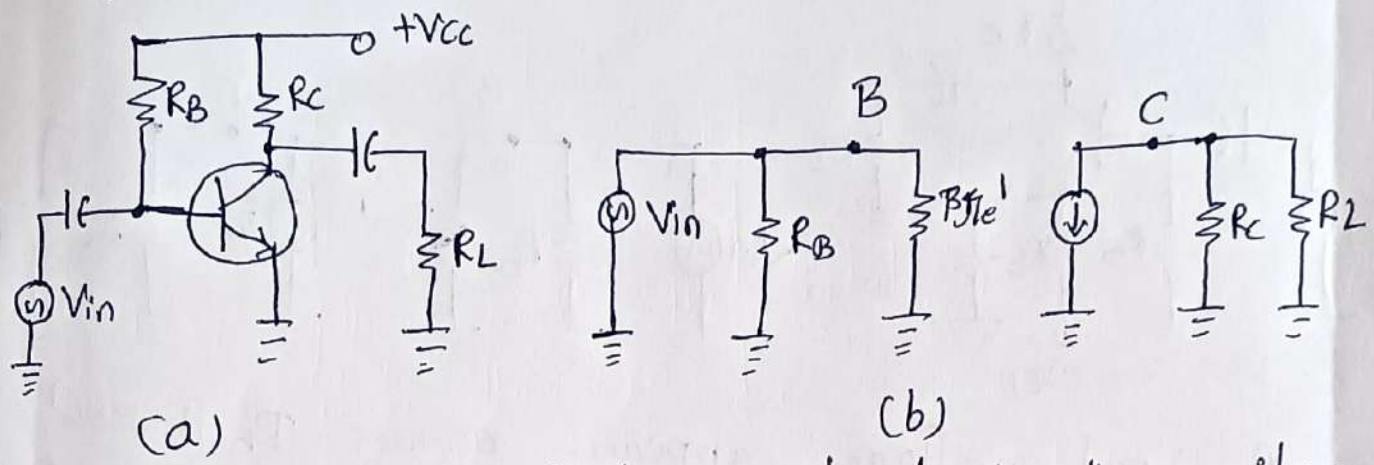
→ To draw an AC equivalent circuit from a given amplifier short circuit all the capacitor and the DC voltage source is ~~shorted~~ circuited to ground & replace the transistor with ac equivalent circuit.

→ ~~Three~~ Four steps for ac equivalent circuits are

i. short all capacitors
ii. DC supply grounded
iii. Replace the transistor by its Π or T model.
iv. Draw the ac equivalent circuit.

I. Base-Biased amplifier (CCE amplifier)

→ Fig shows base-biased amplifier & its ac equivalent circuit.



(a) (b)

→ To get ac equivalent circuit, short all capacitors & dc voltage sources. connect Vcc to ground.

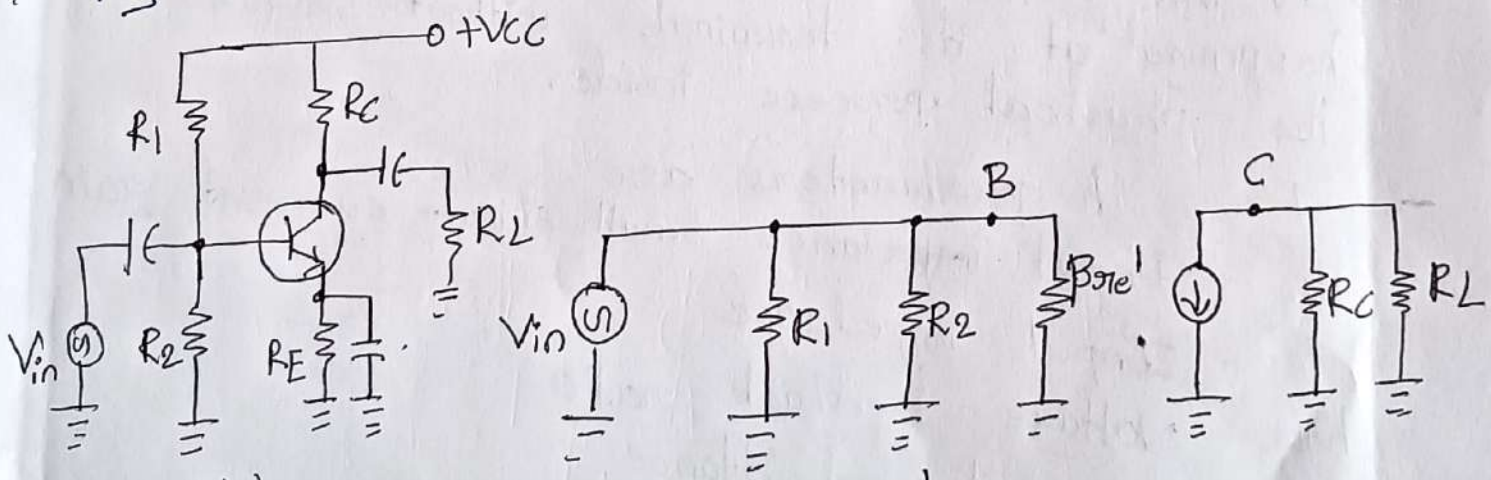
→ Transistor has been replaced by its π model.

→ Vin appears across $R_B \| \beta re'$.

→ ic is the output current through $R_C \| R_L$.

II VDB amplifier (CCE amplifier)

→ Fig shows VDB amplifier & its equivalent circuit.



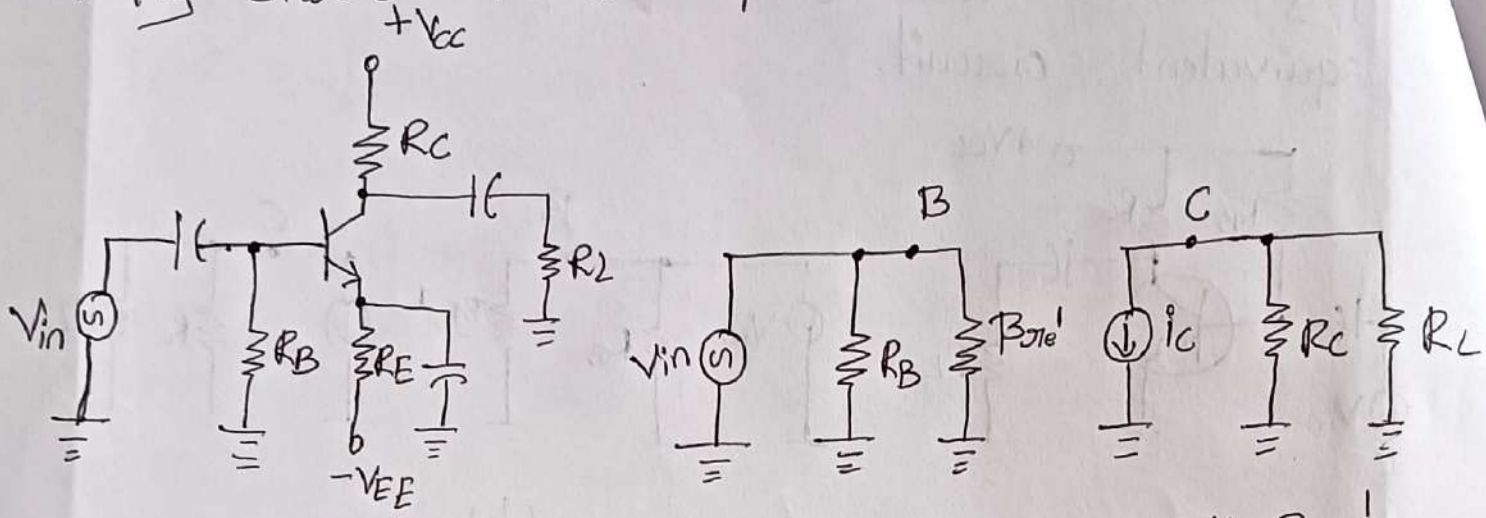
(a) (b).

→ AC i/p voltage appears across $R_1 \| R_2 \| \beta re'$

→ ic jumps through $R_C \| R_L$.

TSEB amplifier

→ Fig shows TSEB amplifier & ac equivalent circu



→ Ac input voltage appears across $R_B \,||\, \beta_{ac} r_e'$

→ The current source pumps an ac current of i_c through $R_c || R_L$.

Ac quantities on the Data sheet

H parameters - When the transistor was 1st invented, an approach known as the h parameters was used to analyze & design transistor circuits.

→ It this method models the transistor on what happening at its terminals without regard for the physical process inside.

→ Four h parameters are.

hfe - ~~Input impedance~~ small signal- current gain

hie - Input impedance

hre - voltage feedback ratio

hoe - output admittance.

Relations between R & H parameters

→ h_{fe} → small signal current gain is identical to the ac current gain

$$\beta = h_{fe}$$

→ h_{ie} → input impedance is equivalent to the input impedance of r_e' parameter

$$r_e' = \frac{h_{ie}}{h_{fe}}$$

→ h_{re} & h_{oe} are not needed for troubleshooting and basic design.

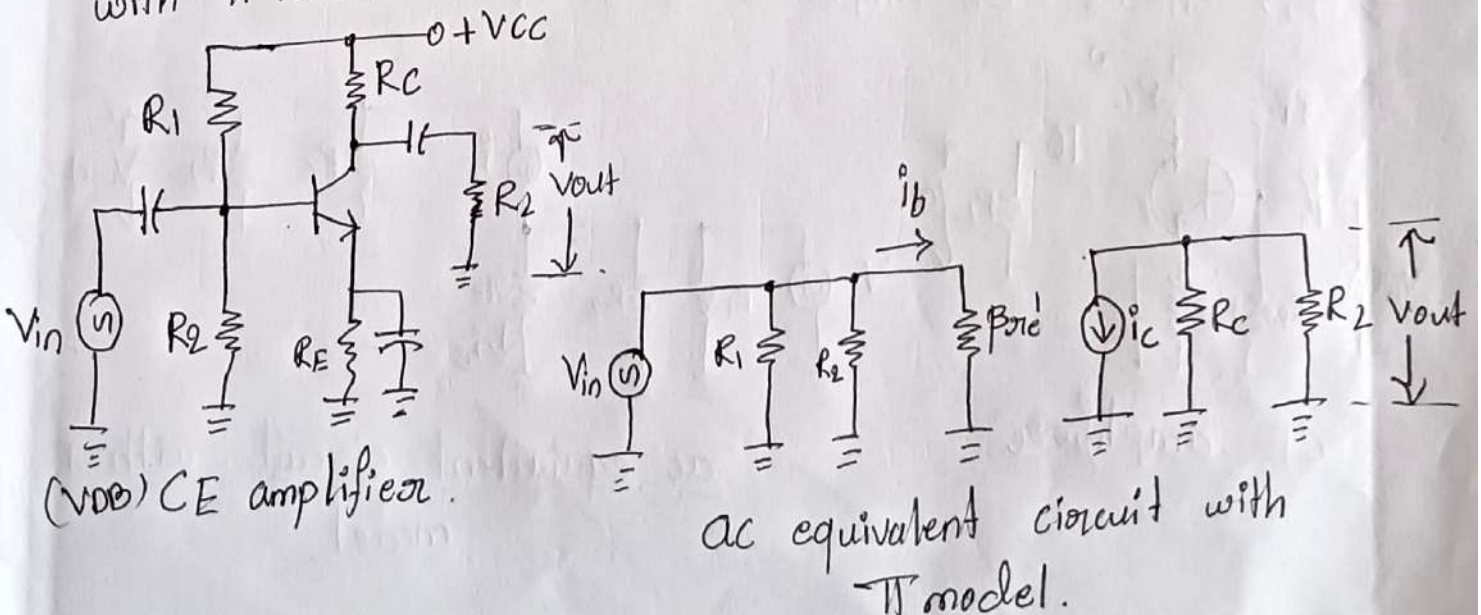
Voltage amplifiers

Voltage gain – It is the ratio of ac output voltage by the ac input voltage. with this concept another equation for voltage gain for trouble shooting.

voltage gain.

I. Derived from the π-model

→ Fig shows (VDB) CE amplifier & its equivalent circuit with π model.



(VDB) CE amplifier.

ac equivalent circuit with π model.

→ The ac base current (i_b) flows through ($\beta r_e'$) according to ohm's law.

$$v_{in} = i_b \beta r_e' \quad \text{—— (1)}$$

→ The current pumpus an i_c through the ($R_C \| R_L$)

$\therefore$ $v_{out} = i_C (R_C \| R_L)$ = $i_c \cong \beta i_b$.

$$v_{out} = \beta i_b (R_C \| R_L) \quad \text{— (2)}$$

from (1) & (2)

$$A_V = \frac{v_{out}}{v_{in}} = \frac{\beta i_b (R_C \| R_L)}{i_b \beta r_e'}$$

$$A_V = \frac{R_C \| R_L}{r_e'} \quad \text{— (3)}.$$

r_c → ac collector resistance is the $R_C \| R_L$.

$\therefore$ $r_c = R_C \| R_L$

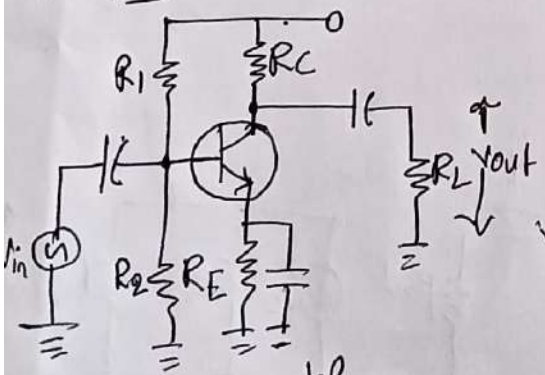
equation (3) can be written as

$$A_V = \frac{r_c}{r_e'}$$

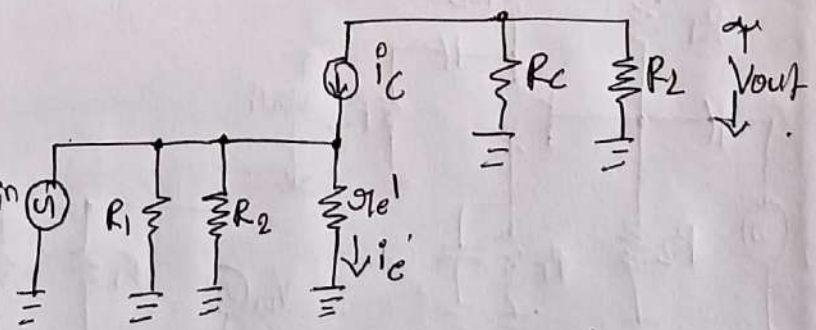
→ The voltage gain equals the ac collector resistance divided by the ac resistance of emitter diode.

II. Voltage gain Derived from the T model

→ Fig shows CE amplifier & ac equivalent circuit with T model



CE amplifier



ac equivalent circuit with T model

→ V_{in} appears across r_e'

$$v_{in} = i_e r_e'$$

→ collector circuit pumps i_c through ac collector resistor r_c $\qquad r_c = R_c \| R_L$

$$\therefore v_{out} = i_c r_c$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{i_c r_c}{i_e r_e'} \qquad i_c \cong i_e$$

$$\therefore \boxed{A_v = \frac{r_c}{r_e'}}$$

→ Both models gives the same equations

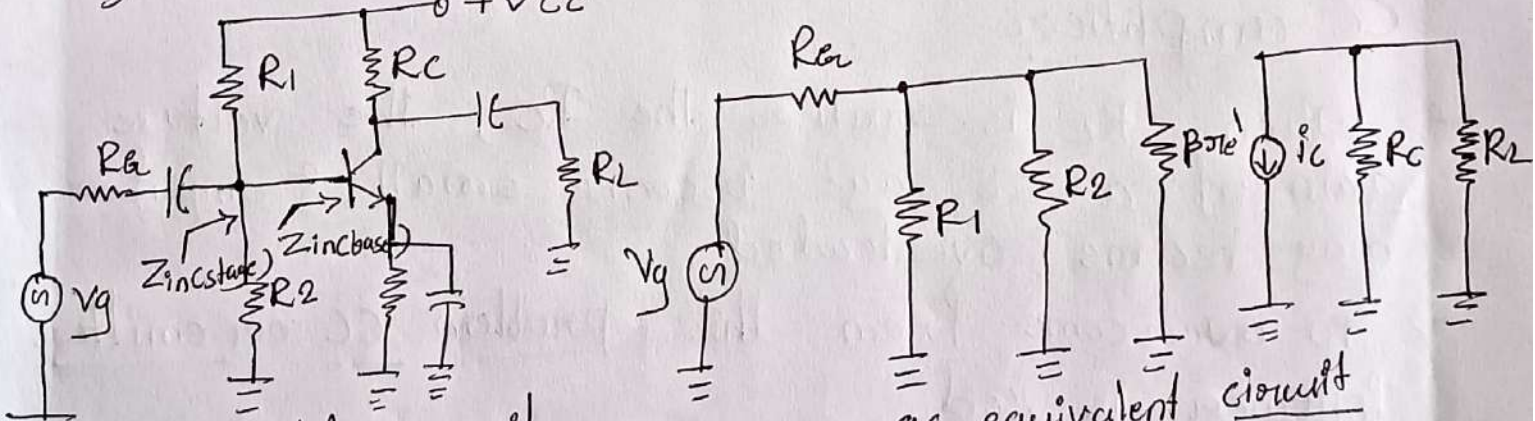
The Loading effect of input impedance.

→ Ideal ac voltage source has zero source resistance.

→ we have an amplifier circuit which reduce the ac voltage appears across emitter (input) diode.

Input impedance

→ Fig shows CE amplifier circuit, ac equivalent circuit & effect of input impedance.



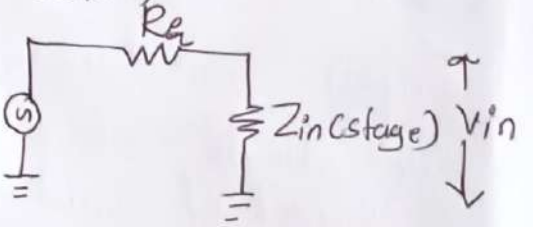
→ V_g (generator ∈ source) voltage)
→ V_g has an internal resistance R_G.
→ When ac generator (source) is not stiff some of the ac source voltage is dropped across R_G.
→ As a result ac voltage between base & ground is less than ideal.
→ AC generator (V_g) has to drive input impedance of the stage $Z_{in(stage)}$.
→ ~~Total~~ $Z_{in(stage)}$ includes effect of $R_1 \| R_2 \| Z_{in(base)}$ [input impedance of the base]
→ ∴ The input impedance of the stage equals

$$Z_{in(stage)} = R_1 \| R_2 \| \beta r_e'$$

Input voltage

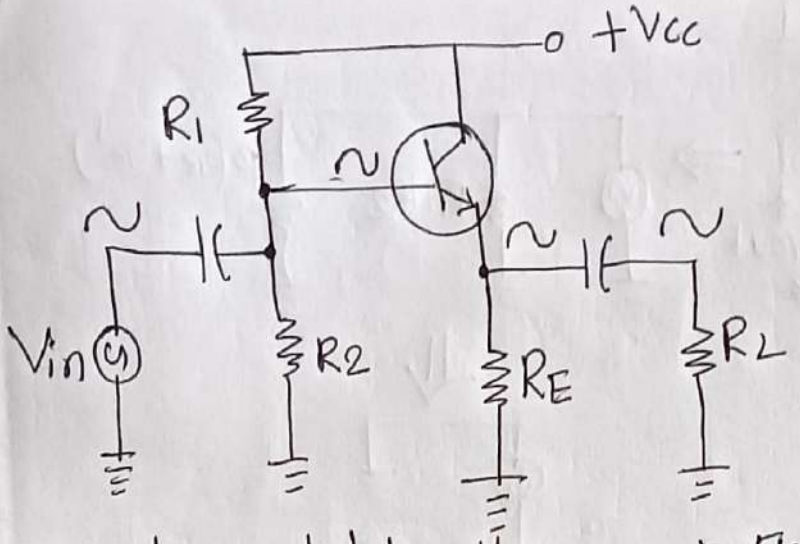
→ when V_g is not stiff, $V_{in} < V_g$ with ~~for~~ voltage divider ~~bi~~ theorem we can write,

$$V_{in} = \frac{Z_{in(stage)}}{R_G + Z_{in(stage)}} V_g$$

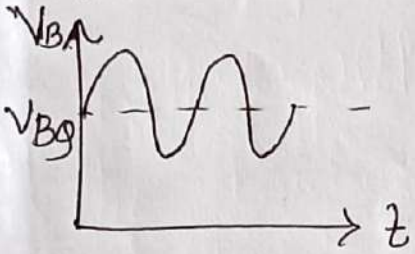


CC amplifier

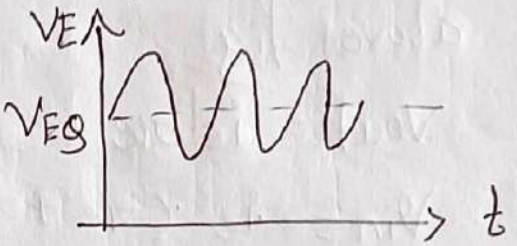
→ When R_L is smaller the R_C, the voltage gain of a CE stage becomes small & amplifier may become overloaded.
→ To overcome from this problem CC or emitter follower is used
→ Fig shows an emitter follower. collector is at ac ground. Input is given to the base terminal output is collected across the emitter terminal.
→ Fig shows emitter follower circuit with waveform.



→ Fig shows total voltage between base & ground which is ac + dc.



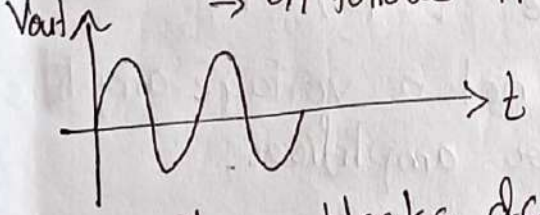
→ Fig shows total voltage between emitter & ground. ac input is centered on V_{EQ}



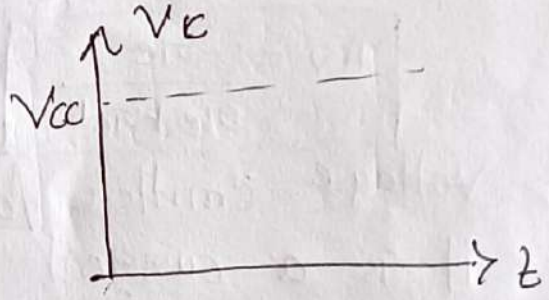
→ Fig shows ac emitter voltage coupled to load.

→ It is inphase & has same amplitude as input voltage. It is pure ac.

→ o/p follows i/p (voltage follower)



→ Fig shows collector voltage. since there is no resistor $V_c = V_{CC}$.



→ capacitor blocks dc.

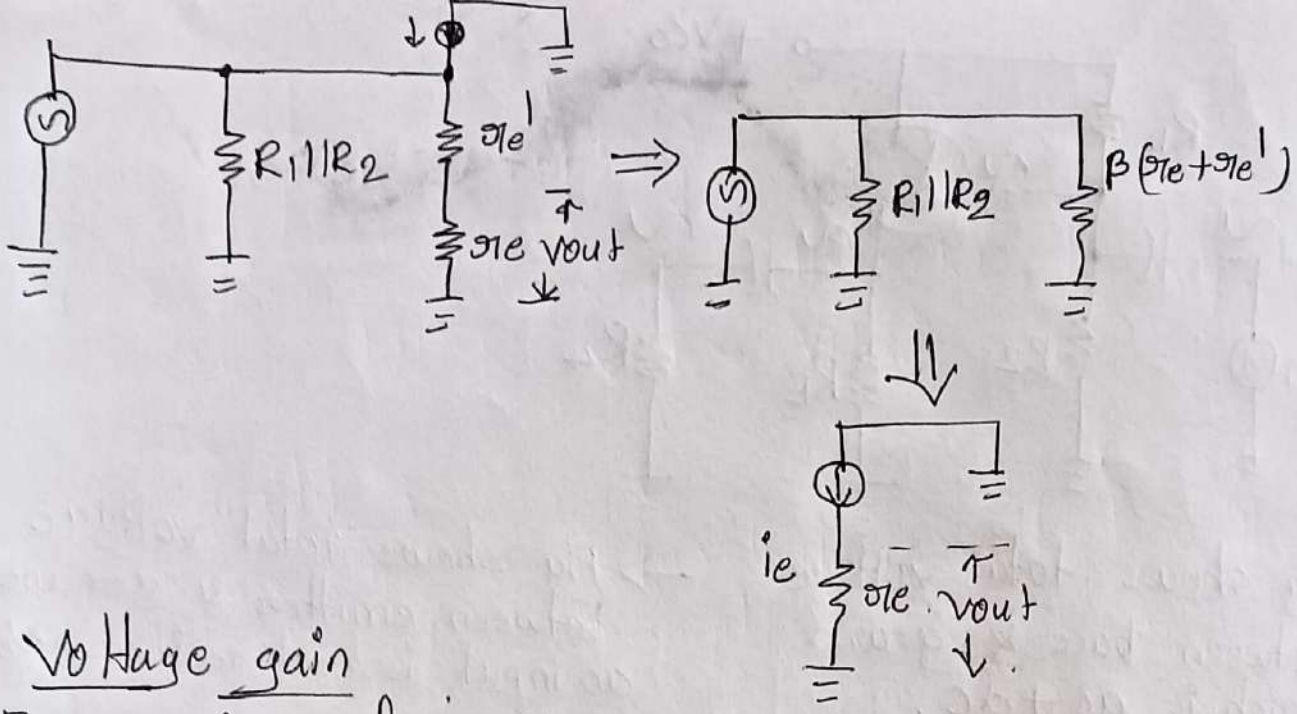
→

→ Negative feedback is used by emitter follower.

→ AC emitter resistance

$$r_e = R_E \,||\, R_2$$ (different from internal r_e')

→ Consider the ac equivalent with T model of emitter follower circuit.



Voltage gain

→ From above fig

$V_{out} = i_e r_e$.

$V_{in} = i_e (r_e + r_e')$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{i_e r_e}{i_e (r_e + r_e')}$$

$$\boxed{A_v = \frac{r_e}{r_e + r_e'}}$$

$r_e \gg r_e'$ $\therefore A_v = 1$.

→ ~~voltage~~ emitter follower is not a voltage amplifier it is a current or power amplifier.

→ Input impedance of the base

$$Z_{in(base)} = \beta (r_e + r_e').$$

Input impedance of the stage

$$Z_{in(stage)} = R_1 \| R_2 \| \beta (r_e + r_e')$$

Output Impedance

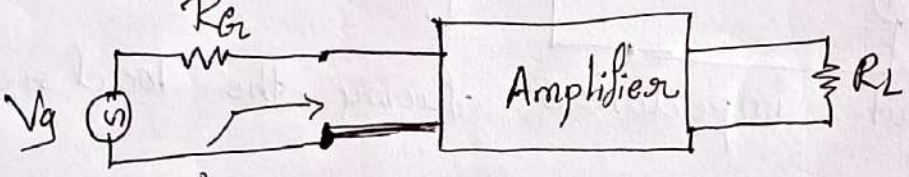
→ Output impedance of an amplifier is the same as its thevenin impedance.

→ Advantage of an emitter follower is its low output impedance.

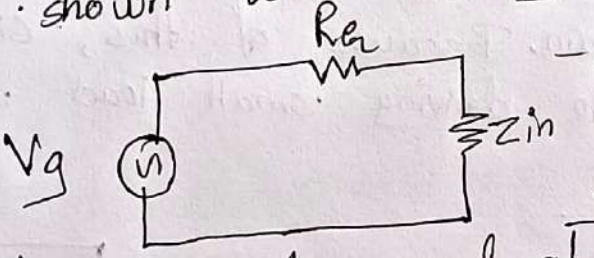
Maximum power transfer occurs when load impedance = source (thevenin) impedance.

For maximum load power is wanted, load impedance ~~match~~ to the output impedance ~~to the outp~~ of an emitter follower.

Fig shows an ac generator driving an amplifier. If the source is not stiff, some of the ac voltage is dropped across the internal resistance R_G.

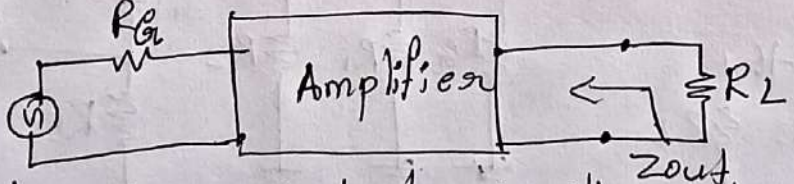


In this case we need to analyze the voltage divider shown below to get input voltage Vin.

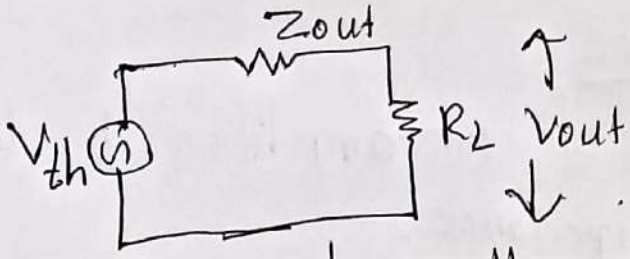


Same idea can be used at output side of the amplifier.

Apply Thevenin theorem at the load terminals.



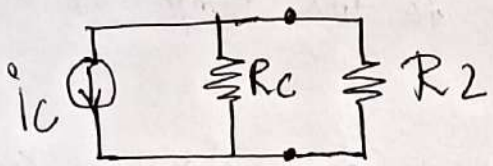
In thevenin equivalent circuit, output impedance forms a voltage divider with R_L, as in fig.



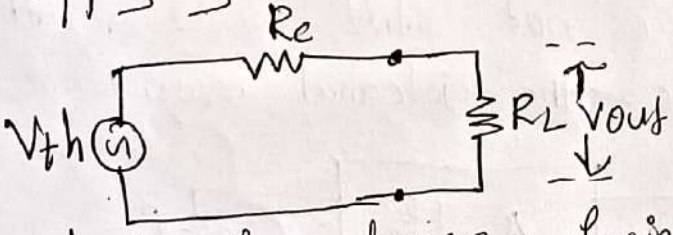
→ if Zout is much smaller than R_2, the output source is stiff & $V_{out} = V_{th}$.

CE Amplifier.

→ Fig. shows the ac equivalent circuit for the output side of CE amplifier



→ After applying thevenin theorem circuit becomes



→ The output impedance facing the load resistance is R_C.

→ voltage gain of CE amplifier depends on R_C a designer cannot make R_C too small without loosing voltage gain. Because of this, CE amplifiers are not suited to driving small load resistances.

Emitter follower.

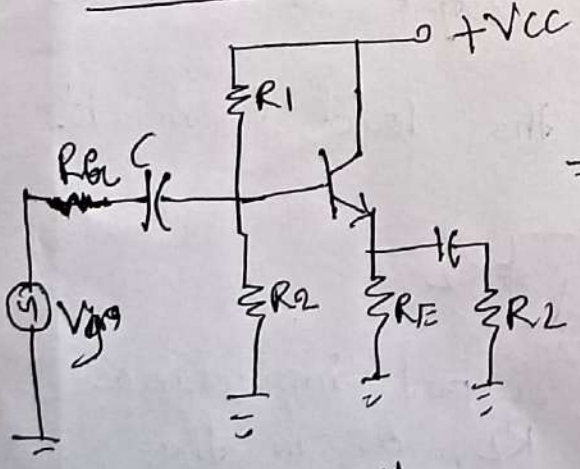


Fig: Emitter follower.

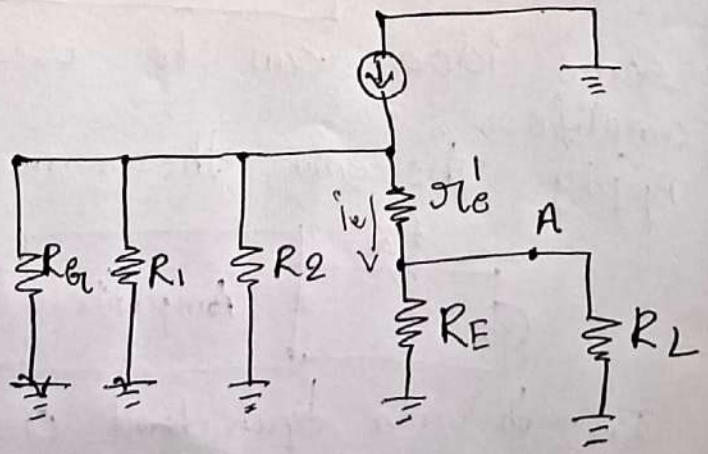
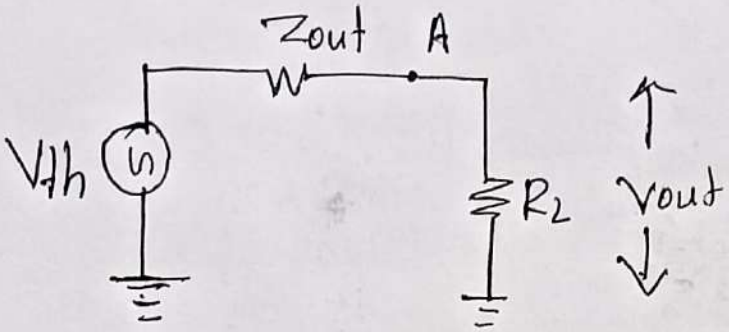


Fig: AC equivalent circuit for emitter follower.

→ When we apply thevenin's theorem to point A, we get



→ The output impedance Zout is much smaller than ~~you can~~ CE amplifier. It equals

$$Z_{out} = R_E \,||\, \left(r_e' + \frac{R_G \,||\, R_1 \,||\, R_2}{\beta} \right)$$

→ The impedance of Base is $R_G || R_1 || R_2$

→ Current gain of the transistor reduces impedance by β.

→ Ideal action - In some designs the biasing resistance & ac resistance of the emitter diode become negligible.

$$\therefore Z_{out} = \frac{R_G}{\beta}$$

→ As a result the emitter follower allows us to build stiff ac sources.

→ Instead of using a stiff ac source that maximizes the load voltage

i,e $Z_{out} << R_L$ (stiff voltage source).

→ A designer may prefer to maximize the load power.

$Z_{out} = R_L$ (Maximum power transfer)

→ In this way, emitter follower can deliver maximum power to a low-impedance load such as stereo speaker.

→ If we remove R_L, circuit acts like a buffer between input & output.

Biasing in MOS amplifier Circuits.

* Essential step in the design of a MOSFET amplifier circuit is establishment of an appropriate dc operating point for the transistor. (this is known as biasing)

* An appropriate dc operating point is characterized by a stable and predictable dc drain current I_D and by a dc drain-to-source voltage V_{DS} that ensures operation in saturation region for all expected input-signal levels.

(I). Biasing by fixing V_{GS}.

* The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide the desired I_D.

* This voltage value can be derived from the power supply voltage V_{DD} through the use of appropriate voltage divider.

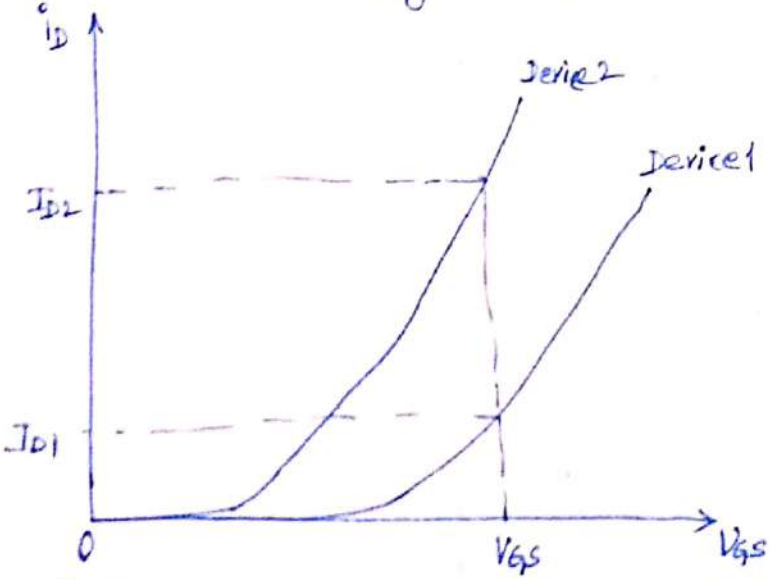
* Alternatively, it can be derived from another suitable reference voltage that might be available in the system

* Independent of how the voltage V_{GS} may be generated, this is not a good approach to biasing a MOSFET.

We have, $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2$

* To understand reason why its not good technique, w.r.t to above eqn.

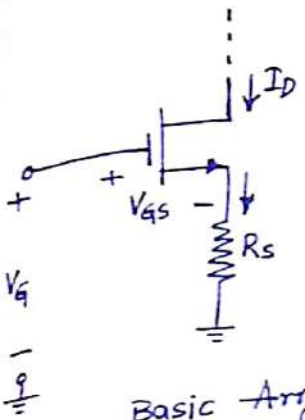
μ_n and V_t depend on temperature, as room temperature varies for same C_{ox}, $\frac{W}{L}$ and V_{GS} values the currents flowing device 1 and device 2 may be different..



The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and Devices 2 represent extremes among units of same type

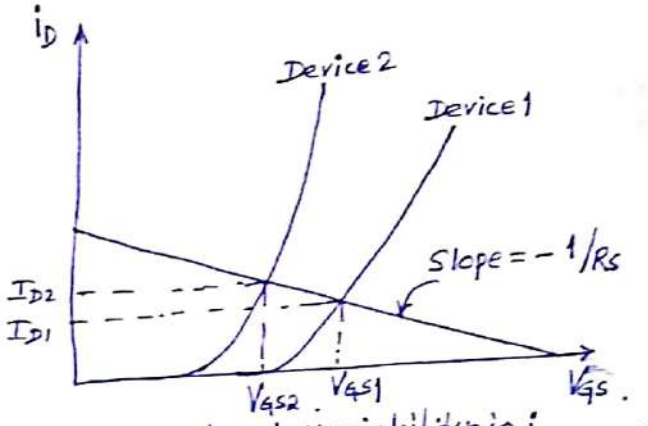
(II) Biasing by fixing V_G and connecting a Resistance in the source

* An excellent biasing technique for discrete MOSFET circuits of fixing the dc voltage at the gate, V_G, and connecting a resistance in the source lead,



Basic Arrangement.

(a). Biasing using fixed voltage at the gate V_G, and a resistance in the source lead



(b) reduced variability in i_D.

For this circuit we can write, $V_G = V_{GS} + R_S \cdot I_D$

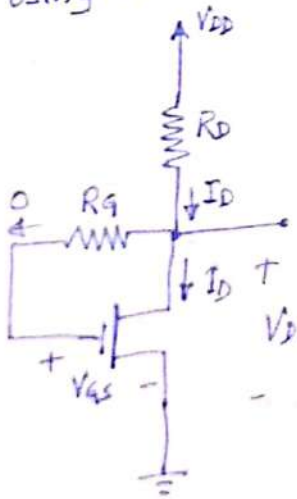
* Now, if V_G is much greater than V_{GS}, I_D will be mostly determined by the values of V_G and R_S.

* However, even if V_G is not much larger than V_{GS}, resistor R_S provides negative feedback, which acts to stabilize the value of bias current I_D.

* $V_G = V_{GS} + R_S I_D$ equation indicates that since V_G is constant, V_{GS} will have to decrease. This inturn results in a decrease in I_D, a change that is opposite to that initially assumed. Thus the action of R_S works to keep I_D as constant as possible.

* The negative feedback action of R_S gives it the name degeneration resistance.

(III). Biasing Using a Drain-to-Gate feedback Resistor



Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G

* Here the large feedback resistance R_G (in MΩ range) forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$). Thus we can write,

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D.$$

which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D$$

* Thus here to I_D changes, say increases, V_{GS} must decrease

* This decrease in V_{GS} in turn causes a decrease in I_D, a change i.e opposite in direction to the one originally assumed

Note:

* Thus the negative feedback or degeneration provided by R_S works to keep the value of I_D as constant as possible

* The above circuit utilized as a CS amplifier by applying input voltage signal to the gate via coupling capacitor, so as not to disturb the dc bias conditions already set up or established.

* The amplified output signal at the drain can be coupled to another part of circuit, again via a capacitor.

Example 1: It is required to design the circuit as shown below to operate at a dc drain current of 0.5mA. Assume $V_{DD} = +5V$. $K_n' W/L = 1 mA/V^2$, $V_t = 1V$ and $\lambda = 0$. Use a standard 5% resistance value for R_D, and give the actual values obtained for I_D and V_D.

Solution Given data $I_D = 0.5mA$

$V_{GS} = V_{DD} - I_D R_D = 5 - 0.5 \times 10^{-3} R_D$.

W.K.T $R_D = \frac{V_{DD} - V_{GS}}{I_D} = \frac{5 - 2}{0.5 \times 10^{-3}} = \frac{3}{0.5 \times 10^{-3}} = 6K\Omega$

To find V_{GS},

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$

$0.5 \times 10^{-3} \times 2 = 1 \times 10^{-3} (V_{GS} - 1)^2$

$V_{GS} - 1 = 1$

$\boxed{V_{GS} = 2V}$ → substituting this value in above eqn. to find R_D we get.

$R_D = 6K\Omega$

So, Let $R_D = 6.2K\Omega$ standard 5% resistance value

To find V_D,

W.K.T $V_D = V_{DD} - I_D R_D$

$V_D = 5 - 0.483 \times 10^{-3} \times 6.2 \times 10^3$

$V_D = 5 - 2.99$

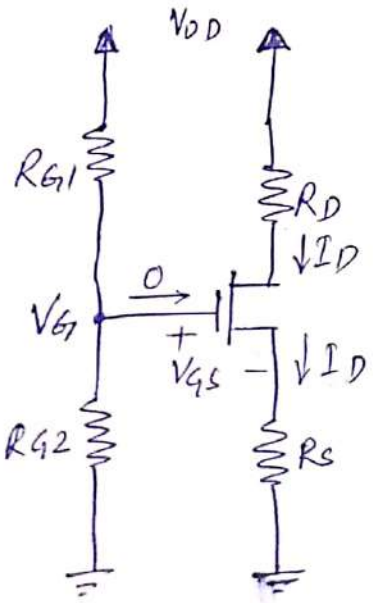
~~$V_D = 1.97V$~~ $\boxed{V_D \cong 2V}$

Example: Since instead of $R_D = 6K\Omega$, we have selected $R_D = 6.2K\Omega$. new value of I_D will be

$$I_D = \frac{V_{DD} - V_{GS}}{R_D} = \frac{5-2}{6.2\times10^3} = \frac{3}{6.2\times10^3} = 0.483mA.$$

Example: It is required to design the circuit of shown below to establish a dc drain current $I_D = 0.5mA$. The MOSFET is specified to have $V_t = 1V$ and $K_n' W/L = 1mA/V^2$. For simplicity, neglect the channel length modulation effect (i.e assume $\lambda = 0$). Use a power-supply $V_{DD} = 15V$. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $K_n' \frac{W}{L}$ but $V_t = 1.5V$.

Solution:



* As a rule of thumb for designing this biasing circuit, we choose R_D and R_S to provide one-third of power supply voltage V_{DD} as a drop across each of R_D, the transistor (i.e V_{DS}) and R_S.

* For $V_{DD} = 15V$, this choice makes $V_D = +10V$ and $V_S = +5V$, since I_D required to be 0.5mA, we can find values of R_D and R_S as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15-10}{0.5\times10^{-3}} = 10K\Omega$$

$$R_S = \frac{V_S}{I_D} = \frac{5}{0.5\times10^{-3}} = 10K\Omega$$

The required value of V_{GS} can be determined by first calculating the overdrive voltage V_{OV} from

$$I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$0.5\times10^{-3} = \frac{1}{2} \times 1\times10^{-3} \times (V_{GS} - 1)^2$$

$$(V_{GS} - 1)^2 = 1$$

$$V_{GS} - 1 = 1$$

$$\boxed{V_{GS} = 2V}$$

Now, since $V_S = +5V$, V_G must be

$$V_G = V_S + V_{GS} = 5 + 2 = 7V$$

* To establish this voltage at the gate we may select $R_{G1} = 8M\Omega$ and $R_{G2} = 7M\Omega$.

* Observe that the dc voltage at the drain (+10V) allows for a positive signal swing of +5V (i.e up to V_{DD}) and a negative signal swing of −4V [i.e down to $(V_G - V_t)$]

* If the NMOS transistor is replaced with another having $V_t = 1.5V$, the new value of I_D can be found as follows:

From current equation.

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad \text{—(1)}$$

We know that $V_G = V_{GS} + I_D R_S$

$$7 = V_{GS} + 10 I_D$$

$$V_{GS} = 7 - 10 I_D \quad \text{—(2)}$$

If we substitute in eqn (1) for V_{GS} from eqn (2) we get

$$I_D = \frac{1}{2}(7 - 10 I_D - 1.5)^2$$

$$2 I_D = (5.5 - 10 I_D)^2$$

$$2 I_D = 5.5^2 + (10 I_D)^2 - 2 \times 10 I_D \times 5.5$$

$$2 I_D = 100 I_D^2 + 30.25 - 110 I_D$$

$$100 I_D^2 - 112 I_D + 30.25 = 0.$$

$$I_D^2 - 1.12 I_D + 0.3025 = 0.$$

Which yields

$$I_D = 0.455 mA$$

$1.4 I_D = 5.5 - 10 I_D$.

$11.4 I_D = 5.5$

$I_D = \frac{5.5}{11.4} =$

Thus change in I_D is

$$\Delta I_D = 0.455 - 0.5 = -0.045 mA$$

which is $\frac{-0.045}{0.5} \times 100 = -9\%$ change

Small-Signal operation and models

* The large-signal operation of common-source MOSFET amplifier, linear amplification can be obtained by biasing the MOSFET to operate in saturation region and by keeping input signal small.

* To study small-signal operation in some detail, we utilize conceptual common-source amplifier circuit

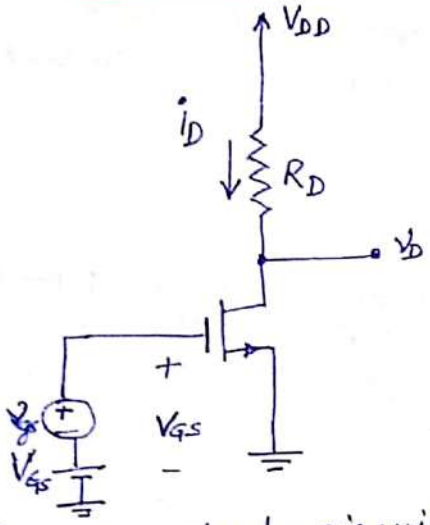


fig. conceptual - circuit

* Here Mos transistor is biased by applying a dc voltage V_{GS},

* Input signal to be amplified v_{gs} is shown superimposed on the dc bias voltage V_{GS}. The output is taken at the drain.

(I) The Dc bias point

* The dc bias current I_D can be found by setting $v_{gs} = 0$; thus.

$$I_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2$$

where we have neglected channel length modulation (i.e $\lambda = 0$).

* The dc voltage at the drain, V_{DS} or simply V_D (since S is grounded) will be,

$$V_D = V_{DD} - I_D R_D$$

* To ensure saturation-region operation, we must have

$$V_D > (V_{GS} - V_t)$$

* Furthermore, since the total voltage at the drain will have a signal component super-imposed on V_D. V_D has to be sufficiently greater than $(V_{GS} - V_t)$ to allow for the required signal swing.

(ii) The Signal current in the Drain Terminal

* Need consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs}$$

resulting in a total instantaneous drain current i_D,

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2$$

$$i_D = \underbrace{\frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2}_{\text{DC bias current}} + \underbrace{K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}}_{\text{current} \propto v_{gs}} + \underbrace{\frac{1}{2} K_n' \frac{W}{L} v_{gs}^2}_{\text{undesirable component, it represents non-linear distortion.}}$$

* To reduce the non-linear distortion introduced by MOSFET, the input signal should be kept small so that

$$\frac{1}{2} K_n' \frac{W}{L} v_{gs}^2 \ll K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

resulting in

$$v_{gs} \ll 2 (V_{GS} - V_t)$$

or equivalently,

$$v_{gs} \ll 2 V_{ov}.$$

where V_{ov} is the overdrive voltage at which transistor operating.

* If the small-signal condition is satisfied, we may neglect the last term & express i_D as

$$i_D = I_D + i_d$$

where

$$i_d = K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

* The parameter that relates i_d and v_{gs} is the MOSFET transconductance, g_m

$$g_m \equiv \frac{i_d}{v_{gs}} = K_n' \frac{W}{L} (V_{GS} - V_t) \quad \text{or} \quad g_m = K_n' \frac{W}{L} V_{ov}$$

* Note that g_m is equal to the slope of the $i_D - v_{GS}$ characteristic at the bias point,

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \bigg|_{v_{GS} = V_{GS}}.$$

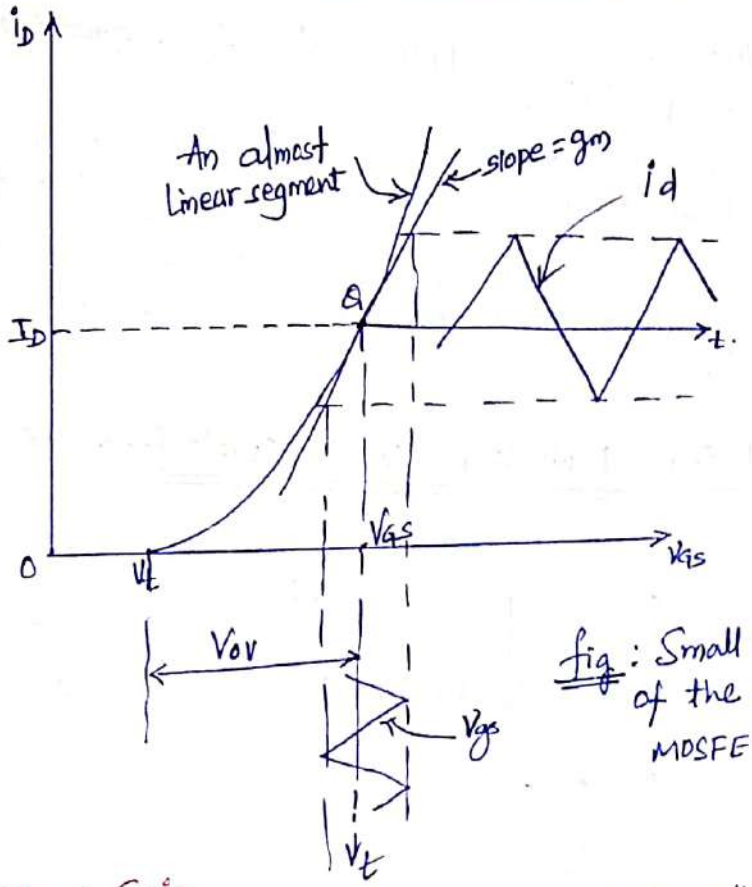


fig: Small signal operation of the enhancement MOSFET amplifier.

(III) The Voltage Gain.

We can express the total instantaneous drain voltage v_D as follows:

$$v_D = V_{DD} - R_D i_D$$

Under the small-signal condition, we have.

$$v_D = V_{DD} - R_D(I_D + i_d)$$

which can be rewritten as.

$$v_D = V_D - \underbrace{R_D i_d}_{\text{signal component } v_d}.$$

$$v_d = -i_d R_D = -g_m v_{gs} R_D.$$

which indicates that voltage gain is given by

$$A_v \equiv \frac{v_d}{v_{gs}} = -g_m R_D$$

"minus" sign indicates 180° phase shift between v_d and v_{gs}.

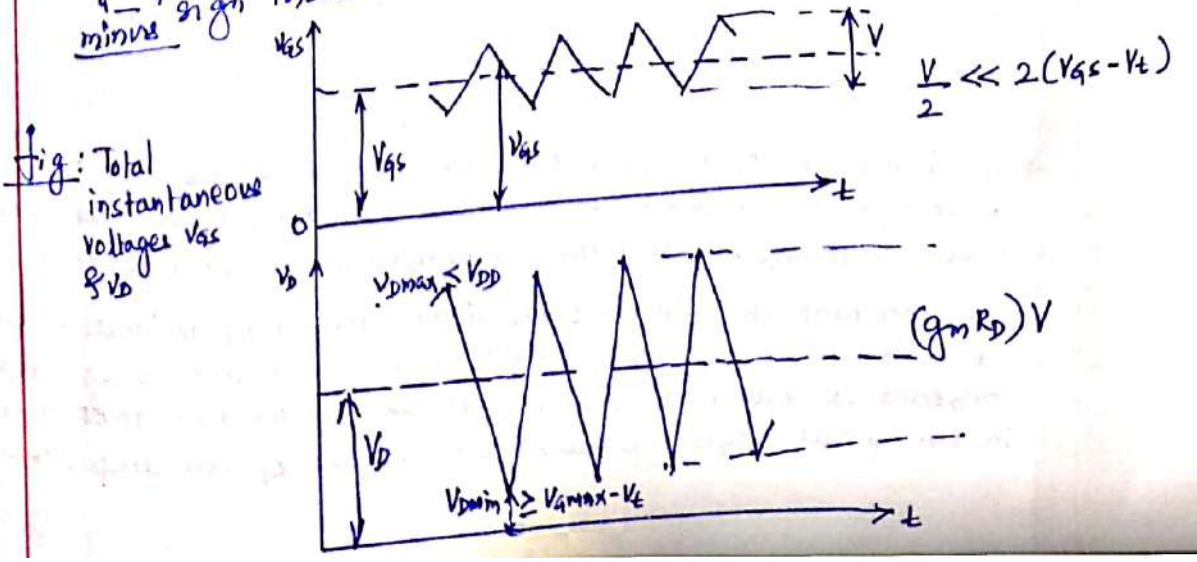
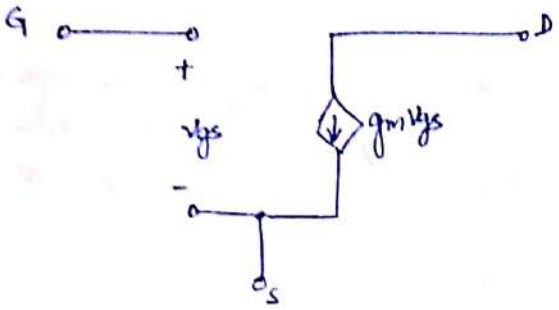


fig: Total instantaneous voltages v_{GS} & v_D

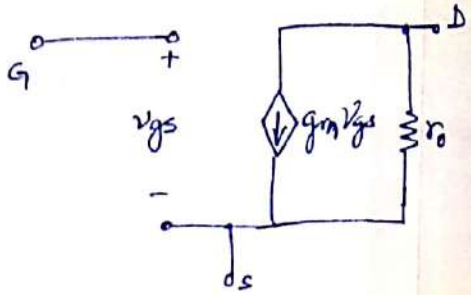
(4) Seperating the DC Analysis and the Signal Analysis.

* Under small-signal approximation, signal quantities are superimposed on dc quantities.
* For instance, total drain current i_D equals the dc current I_D plus the signal current i_d, the total drain voltage $v_D = V_D + v_d$ and so on.
* Once a stable dc operating point has been established and all dc quantities calculated, we may perform signal analysis ignoring dc quantities

(5) Small-Signal Equivalent-Circuit Models for MOSFET



(a)
neglecting dependance of i_D on v_{DS} in saturation (the channel-length modulation effect).



(b)
including the effect of channel length modulation, modeled by output resistance $r_o = |V_A|/I_D$.

* FET behaves as voltage-controlled current source
* It accepts a signal v_{gs}, between gate and source and provides a current $g_m v_{gs}$ at the drain terminal
* The input resistance of this controlled source is very high – ideally infinite.
* The output resistance – that is, a resistance looking into the drain – also high.
* In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent circuit model.
* The rest of the circuit remains unchanged, except that ideal constant dc voltage sources are replaced by short circuits.
* This is a result of the fact that the voltage across an ideal constant dc voltage source does not change, and thus there will always be a zero voltage signal across a constant dc voltage source.
* For constant dc sources: the signal current of an ideal constant dc current soure will always be zero, and thus an ideal constant dc current source can be replaced by an open-circuit in the small signal equivalent circuit of an amplifier

* The circuit resulting can then be used to perform any required signal analysis, such as calculating voltage gain.

* The shortcoming of small-signal model is that it assumes the drain current in saturation is independent of drain voltage

* W.K.T drain current in fact depend on V_{DS} in a linear manner. Such dependance was modeled by a finite resistance r_o between drain and source, where

$$r_o = \frac{|V_A|}{I_D}$$

$V_A = 1/\lambda$ is a MOSFET parameter

I_D = dc drain current without channel length modulation taken into account.

$$\text{i.e. } I_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2 \quad \text{or} \quad \frac{1}{2} \underbrace{\mu_n C_{ox}}_{k_n'} \frac{W}{L} \underbrace{(V_{GS} - V_t)^2}_{V_{OV}}$$

where $k_n' = \mu_n C_{ox}$, $V_{OV} = V_{GS} - V_t$

Typically r_o is in the range of 10KΩ to 1000KΩ. The accuracy of small-signal model can be improved by including r_o in parallel with the controlled source.

* Note g_m and r_o depend on dc-bias point of MOSFET.

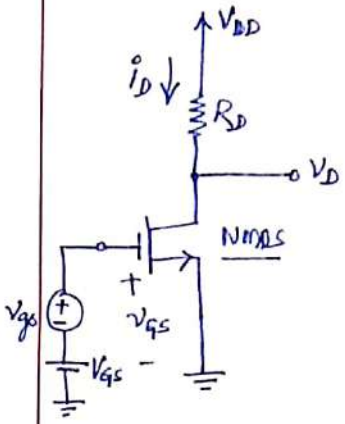
* Voltage gain given by,

$$A_V = \frac{V_d}{V_{gs}} = -g_m (R_D \| r_o).$$

Thus, r_o results in a reduction in the magnitude of voltage gain

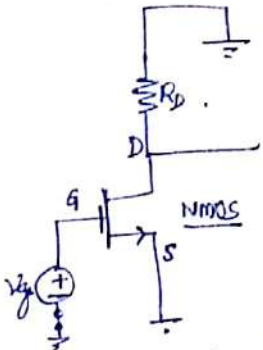
* The analysis above is performed on NMOS transistor.

Example circuit



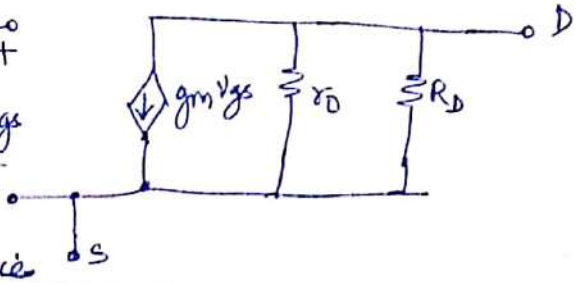
Steps to convert into small signal model.

(I). Replace dc voltage source & capacitors if any present; by a short circuits & current-source by open circuit



(II) Draw small signal model by nMOS. transistor by its equivalent circuit

(III) Voltage gain



* $A_V = \frac{V_d}{V_{gs}} = \frac{-g_m V_{gs} (r_o \| R_D)}{V_{gs}}$

$A_V = -g_m (r_o \| R_D)$

* $Z_i = \infty$ (input ~~resistance~~ impedance)

* $Z_o = r_o \| R_D$ (output impedance)

(6) The Transconductance g_m

* We shall now take a closer look at the MOSFET transconductance given by,

$$g_m = K_n' \frac{W}{L}(V_{GS} - V_t) = K_n' \frac{W}{L} V_{ov}$$

where $K_n' = \mu_n C_{ox}$ and $V_{ov} = V_{GS} - V_t$

Proof.

Note: MOSFET saturation current is given by $I_D = \frac{1}{2} K_n' \frac{W}{L}(V_{GS} - V_t)^2$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

i.e differential expression for I_D w.r.t V_{GS} we get

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1}{2} K_n' \frac{W}{L} 2(V_{GS} - V_t)\ (1-0)$$

$$\boxed{g_m = K_n' \frac{W}{L}(V_{GS} - V_t)}$$ //

* Trans-conductance g_m is directly proportional $K_n' = \mu_n C_{ox}$ and W/L ratio of MOS transistor

* Also, observe that for a given device the transconductance is proportional to the overdrive voltage, $V_{ov} = V_{GS} - V_t$, the amount by which the bias voltage V_{GS} exceeds the threshold voltage V_t.

* Note: However, that increasing g_m by biasing the device at a Larger V_{GS} has the disadvantage of reducing the allowable signal swing at the drain.

* Another useful expression for g_m can be obtained by substituting for $(V_{GS} - V_t)$ by $\sqrt{2I_D / K_n'(\frac{W}{L})}$ we get

we have, $g_m = K_n' \frac{W}{L}(V_{GS} - V_t) = K_n' \frac{W}{L} \sqrt{2I_D / K_n'(\frac{W}{L})}$

$$g_m = \sqrt{2K_n'} \sqrt{W/L} \sqrt{I_D}.$$

This expression shows that

1. For a given MOSFET, g_m is proportional to the square root of the dc bias current.
2. At a given bias current, g_m is proportional to $\sqrt{\frac{W}{L}}$

* Yet another useful expression for g_m of MOSFET can be obtained by substituting for $K_n(W/L)$ by $2I_D/(V_{GS}-V_t)^2$.

we have, $g_m = K_n' \frac{W}{L}(V_{GS}-V_t)$

$$g_m = \left(\frac{2I_D}{(V_{GS}-V_t)^2}\right)\cdot(V_{GS}-V_t) = \frac{2I_D}{V_{GS}-V_t} = \frac{2I_D}{V_{OV}}.$$

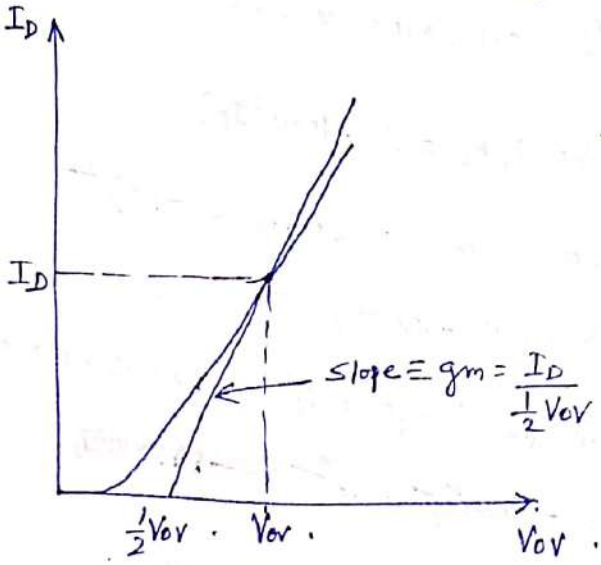


Fig. The slope of tangent at the bias point Q intersects the V_{OV} axis at $\frac{1}{2}V_{OV}$. Thus

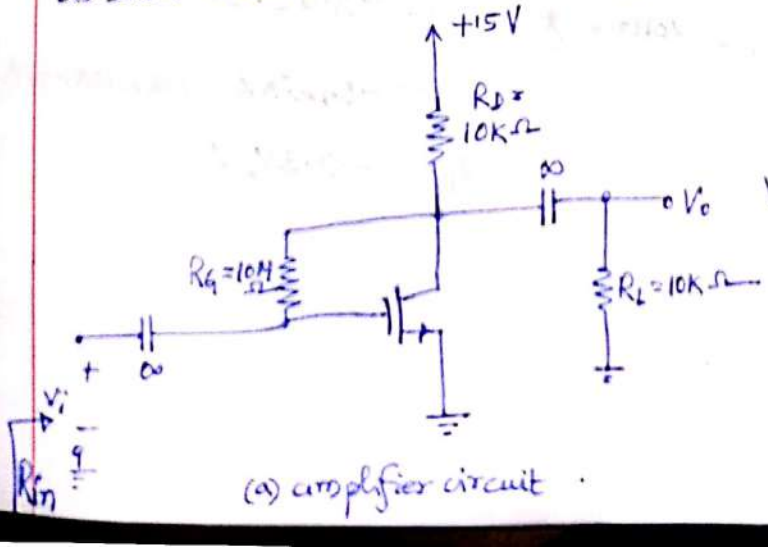
$$g_m = \frac{I_D}{\frac{1}{2}V_{OV}}$$

* Out of three parameters V_{OV}, I_D and $\left(\frac{W}{L}\right)$, designers can choose two parameters independently.

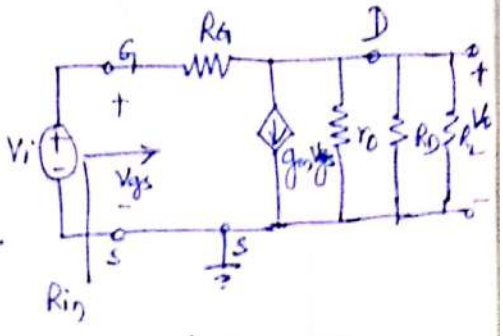
* Eg. designer may choose to operate the MOSFET with certain overdrive voltage V_{OV} and current I_D; the required $\frac{W}{L}$ ratio can then be found and the resulting g_m determined.

Example:

* Figure shows a discrete common-source MOSFET amplifier utilizing the drain-to-gate feedback biasing arrangement. The input signal v_i is coupled to gate via large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor.
* We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal.
* The transistor has $V_t = 1.5\,V$, $K_n'\left(\frac{W}{L}\right) = 0.25\,mA/V^2$ and $V_A = 50\,V$.
* Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.



(a) amplifier circuit.



(b) equivalent-circuit model.

olution

We first evaluate the dc operating point as follows:

$$I_D = \frac{1}{2} \times 0.25 \times 10^{-3} (V_{GS} - 1.5)^2$$

* For simplicity, we have neglected the channel-length modulation ($\lambda = 0$). Since the dc gate current is zero, there will be no dc voltage drop across R_G: thus $V_{GS} = V_D$.

$$I_D = 0.125 \times 10^{-3} (V_D - 1.5)^2$$

Also,

$$V_D = V_{DD} - I_D R_D = (15 - 10 \times 10^3 I_D).$$

$$I_D = 0.125 \times 10^{-3} (15 - 10 \times 10^3 I_D - 1.5)^2$$

$$8 \times 10^3 I_D = (13.5 - 10 \times 10^3 I_D)^2$$

$$8 \times 10^3 I_D = (13.5)^2 + (10 \times 10^3 I_D)^2 - 2 \times 13.5 \times 10 \times 10^3 I_D$$

$$0 = 10000 I_D^2 + 13.5^2 - 262 \times 10^3 I_D$$

Solving.

$I_D = 1.06 mA$ & $V_D = 4.4V$

(Note: that other solution of quadratic equation is not physically meaningful.)

* The value of g_m is given by, $g_m = K_n' \frac{W}{L} (V_{GS} - V_t)$

$$g_m = 0.25 \times 10^{-3} (4.4 - 1.5)$$

$$g_m = 0.725 mA/V$$

* The output resistance r_o is given by, $r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = 47 K\Omega$

* $v_o \cong -g_m v_{gs} (R_D \| R_L \| r_o)$

Since $v_{gs} = v_i$, the voltage gain $A_v = -g_m (R_D \| R_L \| r_o)$

$$= -0.725 \times 10^{-3} (10K \| 10K \| 47K)$$

$$A_v = -3.3 V/V.$$

* To evaluate the input resistance R_{in}, we note that the input current i_i is given by,

$$i_i = (v_i - v_o)/R_G$$

$$i_i = \frac{v_i}{R_G}\left(1 - \frac{v_o}{v_i}\right)$$

$$\hat{i}_i = \frac{\hat{v}_i}{R_G}\left(1 - (-3.3)\right)$$

$$i_i = \frac{4.3\,v_i}{R_G}$$

Thus, $R_{in} = \frac{v_i}{i_i} = \frac{R_G}{4.3} = \frac{10\times10^6}{4.3} = 2.33\,M\Omega$

* The largest allowable input signal $\hat{v}_i$ is determined by the need to keep MOSFET in saturation at all times; that is,

$$v_{DS} \geq v_{GS} - V_t$$

Enforcing this condition, with equality, at the point v_{GS} is maximum and v_{DS} correspondingly minimum, we write

$$v_{DSmin} = v_{GSmax} - V_t.$$

$$V_{DS} - |A_v|\hat{v}_i = V_{GS} + \hat{v}_i - V_t.$$

$$4.4 - 3.3\hat{V}_i = 4.4 + \hat{V}_i - 1.5$$

$$\boxed{\hat{V}_i = 0.34\,V.}$$

Note that: in the negative direction, this input signal amplitude results in $v_{GSmin} = 4.4 - -0.34 = 4.06\,V$, which is larger than V_t. and thus transistor remains conducting.

* Thus, as the limitation on input signal amplitude is posed by the upper-end considerations, and the maximum allowable input signal peak is 0.34 V

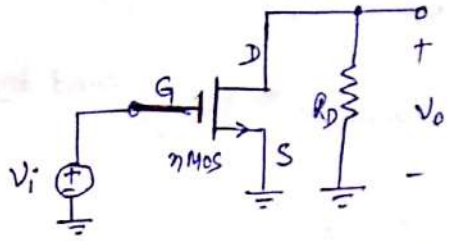
※ End of Module 1 ※.

Module 2 * MOSFET Amplifier configuration.

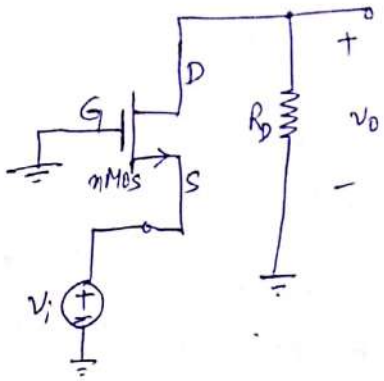
* MOSFET internal capacitances and High frequency model
* Frequency response of the CS amplifier
* Oscillators.

MOSFET Amplifier Configuration.

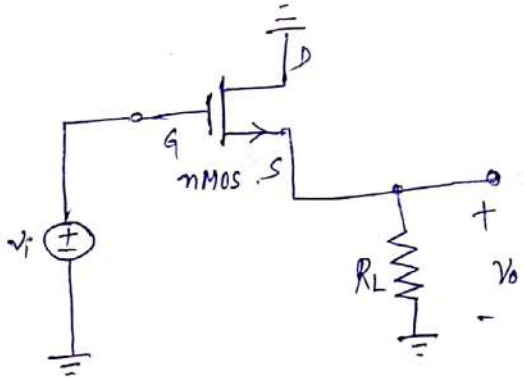
Three Basic configurations:



(a) Common-Source (CS)

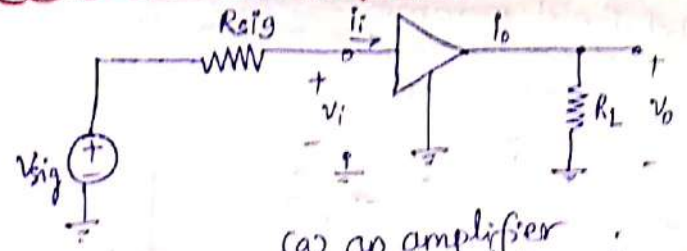


(b) Common-Gate (CG)



(c) Common-Drain (CD)

Characterising Amplifiers:

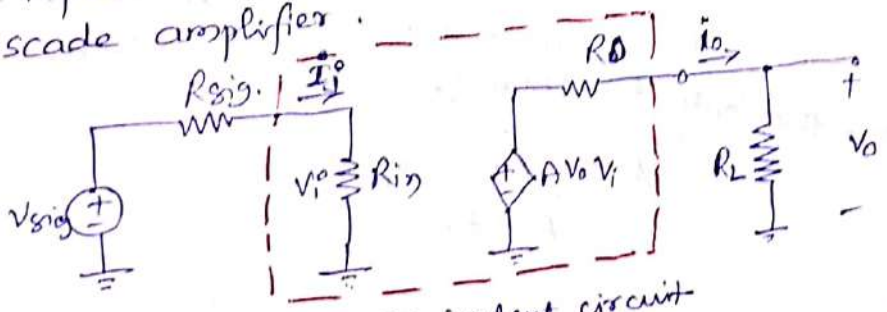


(a) an amplifier.

* Above figure shows an amplifier fed with a signal source having an open-circuit voltage V_{sig} and an internal resistance R_{sig}.

* These can be parameters of actual signal source or, in a cascade amplifier, the Thevenin equivalent of the output circuit of another amplifier stage preceding the one under study.

* The amplifier is shown with a load resistance R_L connected to the output terminal. Here, R_L can be actual load resistance or the input resistance of a succeding amplifier stage in a cascade amplifier.



(b) equivalent circuit

* Fig (b) shows the amplifier circuit with the amplifier block replaced by its equivalent-circuit model.

* The input resistance R_{in} represents the loading effect of the amplifier input on the signal source.

we get, $R_{in} = \frac{v_i}{i_i}$ & together with R_{sig} forms voltage divider that reduces V_{sig} to the value v_i that appears at the amplifier input,

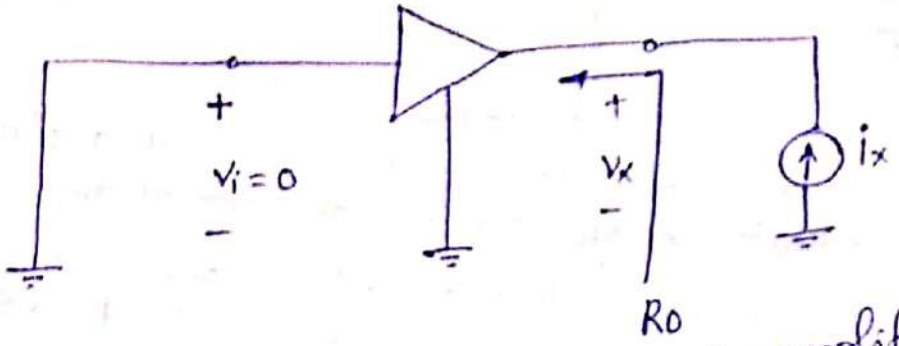
$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} \cdot V_{sig} \quad \text{— (A)}$$

* All the amplifier circuit studied in this section are "unilateral", i.e they do not contain internal feedback. & this, R_{in} will be independent of R_L.

* The second parameter in characterising amplifier performan is the open-circuit voltage gain A_{vo}, defined as.

$$A_{vo} \equiv \left. \frac{v_o}{v_i} \right|_{R_L = \infty}$$

* The third and final parameter is the output resistance R_o, is the resistance seen looking back into the amplifier output terminal with v_i set to zero.



(C) Determining the amplifier output resistance

* Thus R_o can be determined, ~~at~~ $R_o = \frac{v_x}{i_x}$

* The controlled source $(A_{vo} \cdot v_i)$ and the output resistance R_o represent the Thevenin equivalent of the amplifier output circuit, and the output voltage v_o can be found from,

$$v_o = \frac{R_L}{R_L + R_o} A_{vo} \cdot v_i$$

Rearranging above eqn we get

Voltage gain of amplifier

$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_L + R_o} \cdot A_{vo} \quad \text{— (B)}$$

* overall voltage gain G_v, $G_v = \frac{v_o}{v_{sig}}$

by combining eqn (A) & (B)

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} \cdot A_{vo} \cdot \frac{R_L}{R_L + R_o}$$

The Common-Source Amplifier without R_s (source resistance)

* Common-source configuration is most widely used MOS amplifier configuration.

capacitors & dc supply short circuited & re drawn the ckt we get fig (a)

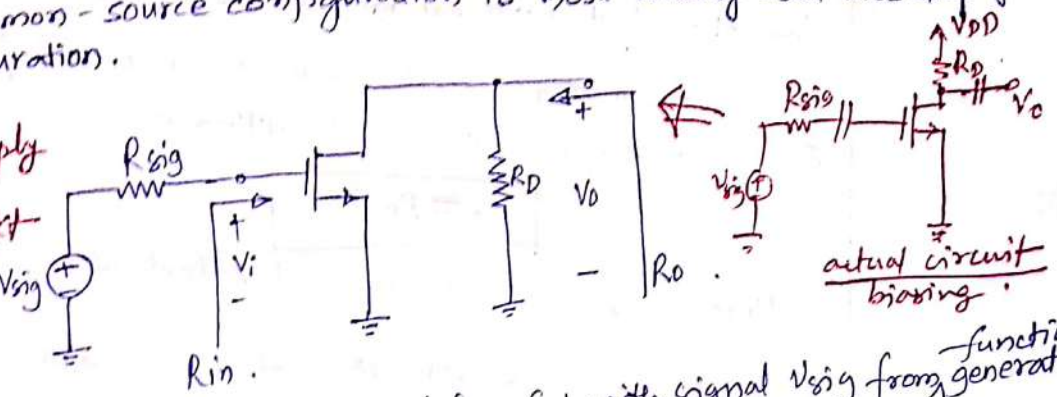


fig (a) Common-Source (CS) amplifier fed with signal V_{sig} from function generator with a resistance R_{sig}. The bias circuit is omitted.

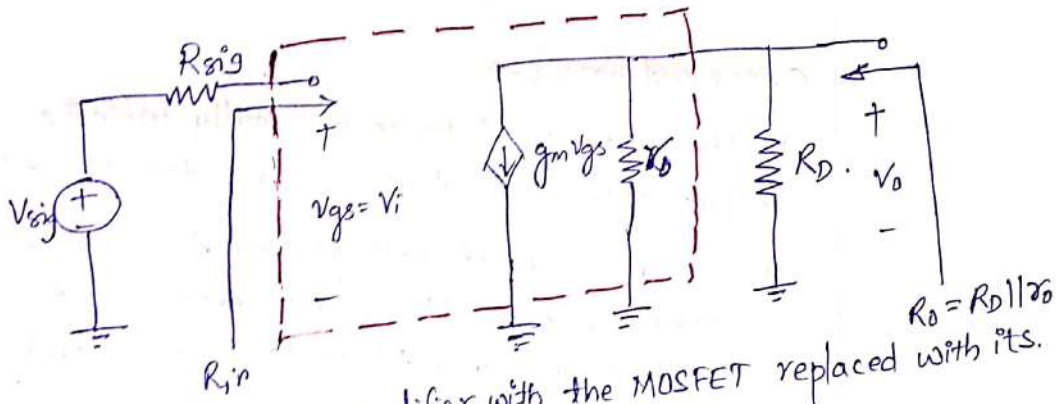


fig (b) The common-source amplifier with the MOSFET replaced with its hybrid-π model.

* Input Resistance, $R_{in} = \infty$.

* The output voltage V_o is found by multiplying the current ($g_m V_{gs}$) by the total resistance between the output node & ground,.

$$V_o = -(g_m V_{gs})(R_D \| r_o)$$

Since $v_{gs} = v_i$, the open circuit voltage gain $A_{vo} \equiv \frac{V_o}{V_i}$ can be obtained as, $A_{vo} = -g_m(R_D \| r_o)$.

* r_o, reduces the voltage gain. In discrete-circuit amplrs, R_D is much lower than r_o, and the effect of r_o reducing $|A_{vo}|$ is less than 10% or so.

* Thus in many cases we can neglect r_o and express Avo simply as, $A_{vo} = (-g_m R_D)$

imp Neglecting r_o is allowed in discrete-circuit design only.

* The output resistance R_o is the resistance seen looking back into the output terminal with v_i set to zero.

* We see from fig ⓑ that with v_i set to zero, v_{gs} will be zero, & thus $g_m v_{gs}$ will be zero, resulting in

$$R_o = R_D \| r_o$$

Here, r_o has the beneficial effect of reducing the value of R_o.

* In discrete circuits, this effect is slight & we can make the approximation.

$$R_o \simeq R_D$$

Observations :⇒

1. * The input resistance is ideally infinite.
2. * The output resistance is moderate to high.
3. * The open-circuit voltage gain A_{vo} can be high, making CS configuration the work-horse in MOS amplifier design. However bandwidth is less in CS configuration.

Overall voltage gain $G_v = \frac{v_o}{v_i} = \frac{v_o}{v_{gs}}$.

* Infinite R_{in} will make entire signal v_{sig} appear at the amplifier input,

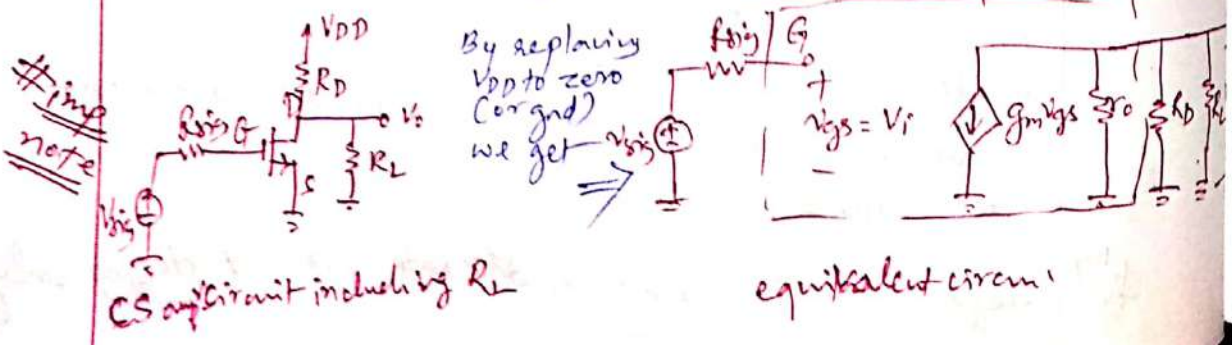
$$v_i = v_{sig}$$

* If a load resistance R_L is connected to the output terminal of the amplifier, this resistance will come in parallel with R_D.

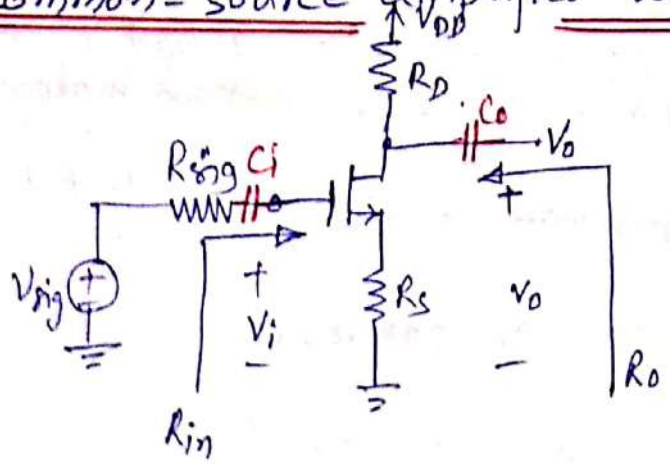
* Voltage gain $A_v = -g_m (r_o \| R_D \| R_L)$

* Overall voltage gain $G_v = A_v$ because in this case $v_{sig} = v_i$

$$\text{So } G_v = -g_m (r_o \| R_D \| R_L)$$



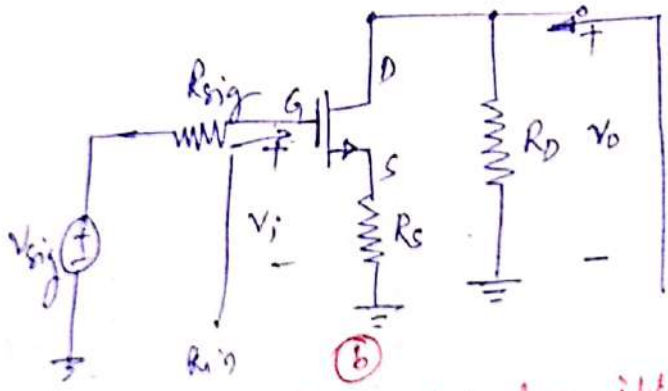
Common-source amplifier with a Source Resistance



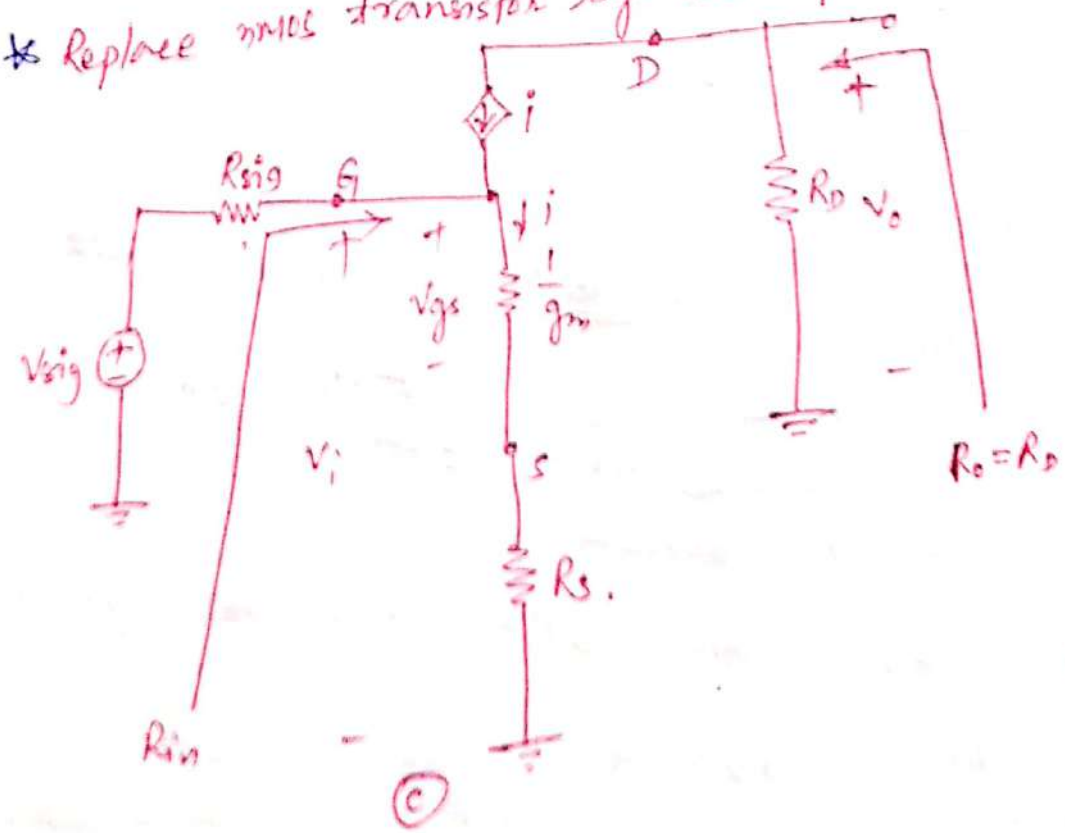
C_i, C_o - coupling capacitors.

(a)

* To convert into small-signal equivalent model
  make $V_{DD} = 0V$ or gnd & capacitors short circuited



* Replace nMOS transistor by it's equivalent model we get,



* It should be noted that we have not included r_o in the equivalent circuit model to simplify analysis, & effect of r_o on discrete-circuit amplifier is not important.

* From fig.(c) input resistance R_{in} is infinite and thus $R_{in} = \infty$ and thus $V_i = V_{sig}$;

* Here fraction of V_i appears between gate & source as V_{gs}.

* It can be determined from voltage devider composed of $1/g_m$ and R_s that appears across the amplifier input as follows,

$$V_{gs} = V_i \frac{1/g_m}{1/g_m + R_s} = \frac{V_i}{1 + g_m R_s}$$

* Note: We can use the value of R_s to control magnitude of V_{gs} & thereby ensure V_{gs} doesnot become too large and cause unacceptably high non-linear distortion.

* One more advantage of R_s, is it increases allowable bandwidth of input signal.

* The output voltage V_o is obtained by multiplying the controlled-source current i by R_D,

$$V_o = -iR_D$$

$$V_o = -\left(\frac{V_i}{1/g_m + R_s}\right) R_D \quad \left[\because i = \frac{V_i}{1/g_m + R_s}\right]$$

Open-Circuit Voltage gain.

$$A_{v_o} = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_s}$$

* By including R_s, it reduces gain by $(1 + g_m R_s)$
* By same factor $(1 + g_m R_s)$ bandwidth will improve.
* Because of negative feedback action of R_s it is known as source-degeneration resistance.

* Output Resistance $R_o = R_D$.

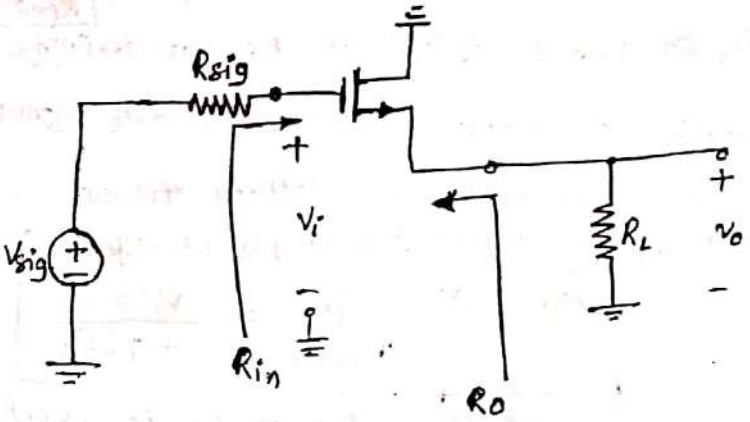
* Considering R_L - load resistance connected at the output.

* output resistance $R_o = R_D \| R_L$

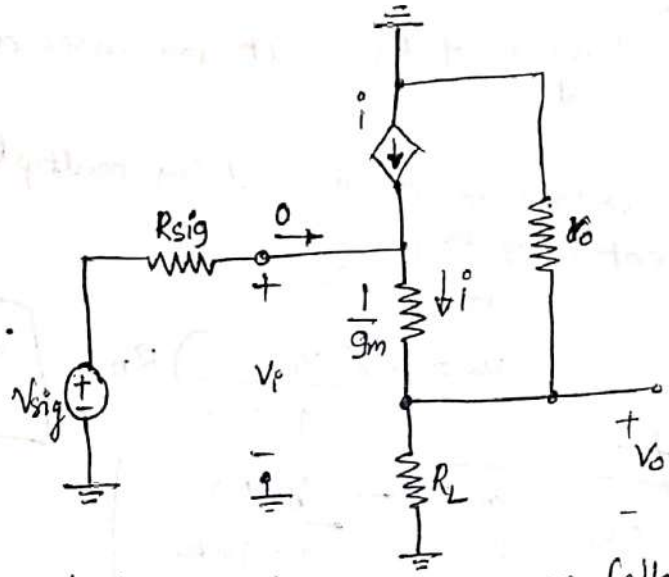
* Voltage gain

$$A_v = \frac{R_D \| R_L}{1/g_m + R_s} \quad \text{or} \quad \frac{g_m (R_D \| R_L)}{1 + g_m R_s}$$

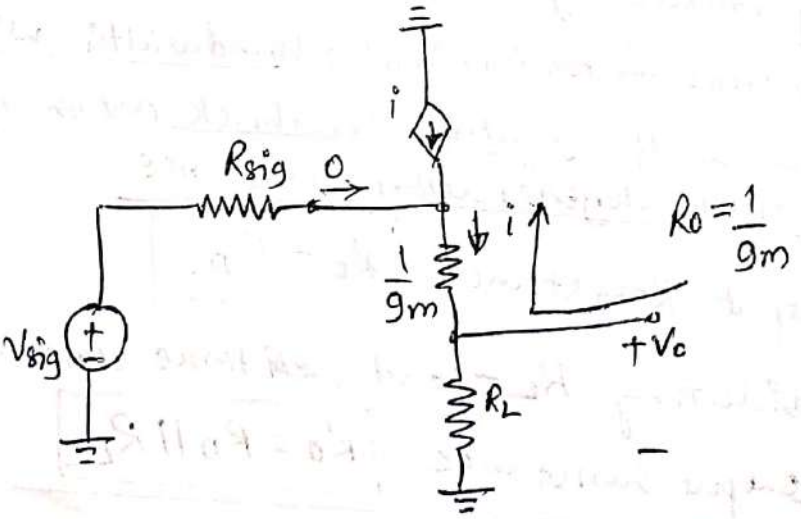
The Common-Drain Amplifier or Source Follower.



(a) Common-drain amplifier or source follower.



(b) Equivalent circuit of the source follower obtained by replacing the MOSFET with it's T model.



(c) In discrete circuits $r_o \gg R_L$, neglecting r_o, we obtai simplified equivalent circuit.

* The source-follower is fed with a signal generator and has a R_L between source terminal & ground.

* R_L includes both actual load and any other resistance that may be present between a source terminal & ground.

* T model is more convenient to use as R_L is connected in source terminal.

* $R_{in} = \infty$.

and $A_V \equiv \frac{V_o}{V_i} = \frac{R_L}{R_L + 1/g_m}$

setting $R_L = \infty$ we obtain.

$$\boxed{A_{V_0} = 1.}$$

* The output resistance R_o is found by setting $V_i = 0$ (i.e by grounding gate).

* $R_o = 1/g_m$, Looking back into output terminal, excluding R_L we have this.

* The unity open-circuit voltage gain together with R_o can be used to find when a load resistance R_L connected.

* Because $R_{in} = \infty$, $V_i = V_{sig}$, and the overall voltage gain is.

$$G_V = A_V = \frac{R_L}{R_L + 1/g_m}$$

$1/g_m$ is usually low, so $G_V \cong 1$ (unity gain)

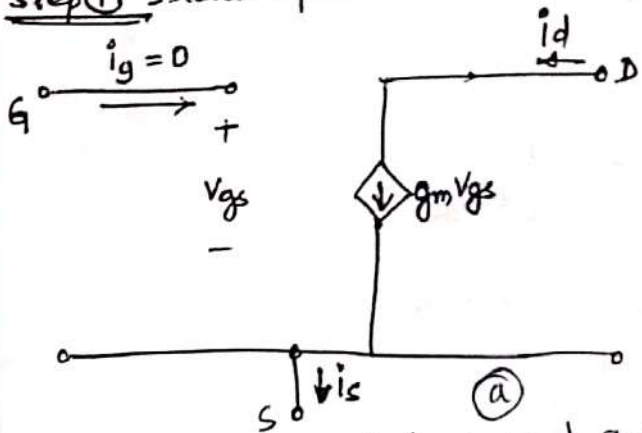
Note:

* Very high input resistance (ideally ∞)
* Low output resistance &
* open-circuit voltage gain near unity (ideally, unity)

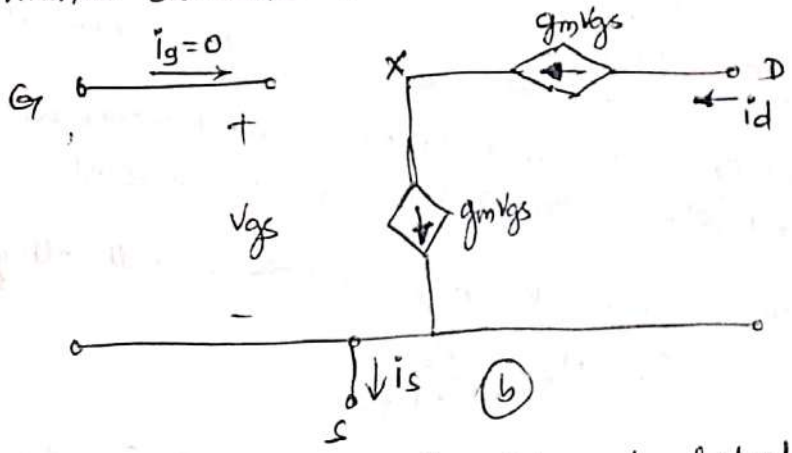
The T equivalent-circuit model

* Through a simple circuit transformation it is possible to develop an alternative equivalent circuit model for MOSFET, known as T model.

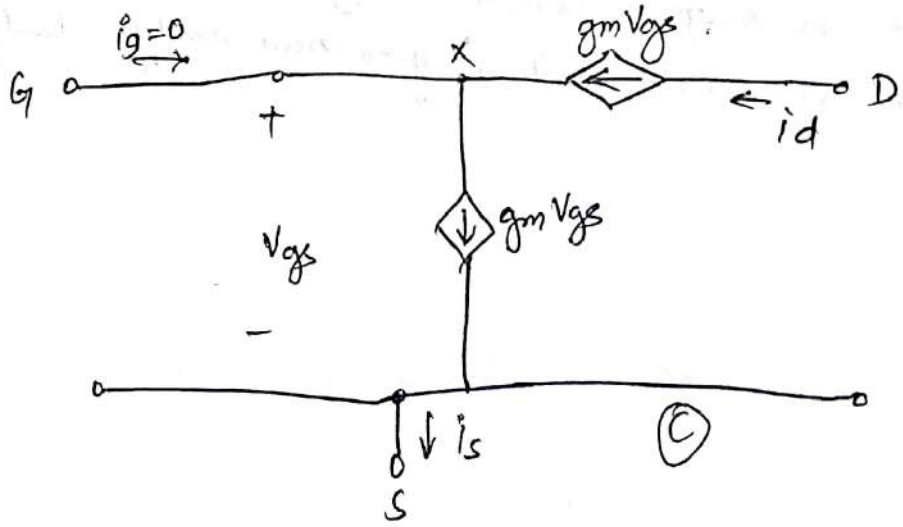
step① shows equivalent circuit for MOSFET without r_o.



step② We have added second $g_m V_{gs}$ current source in series with the original controlled source. This addition doesnot change terminal currents & is allowed.

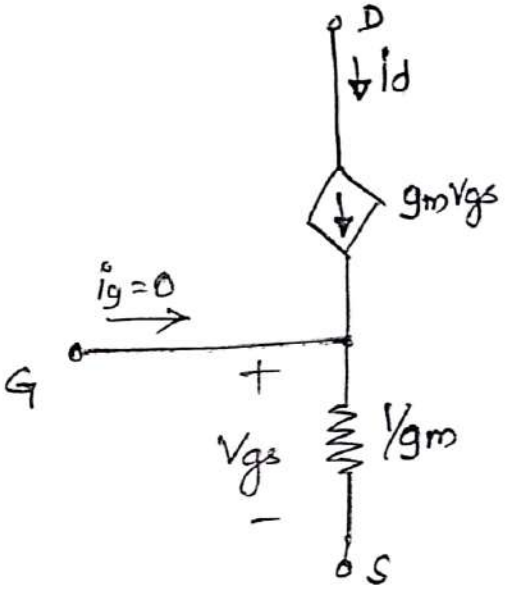


step③ The newly created circuit node, labelled x, is joined to the gate terminal G. Observe that the gate current doesnot change i.e, it remains equal to zero - and thus this connection doesnot alter terminal characteristics.



Step 4: Controlled current source $g_m v_{gs}$ connected across its control voltage v_{gs}. We can replace controlled source by resistance as long as this resistance draws an equal current as the source. Thus, the value of resistance is $v_{gs}/g_m v_{gs} = 1/g_m$.

* which depicts alternative model. Observe that i_g is still zero, $i_d = g_m v_{gs}$, and $i_s = v_{gs} / 1/g_m = g_m v_{gs}$, all same as fig (a).



(d) T equivalent model of MOSFET.